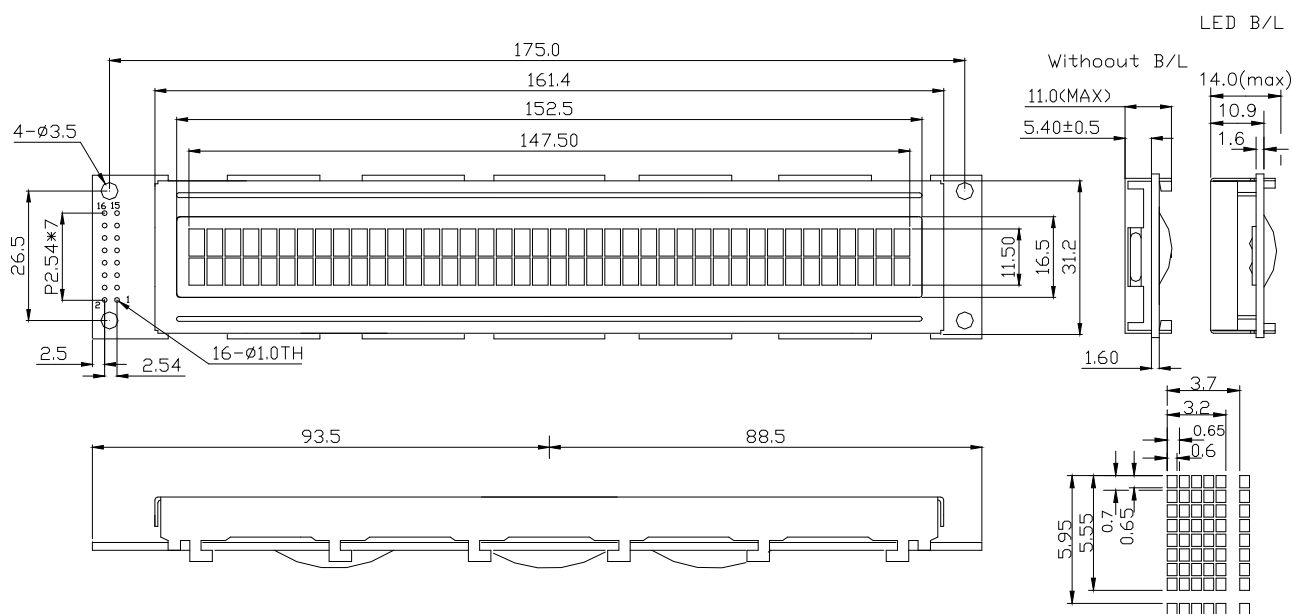


## Features

1. 5x8 dots
2. Built-in controller (ST7066 or equivalent)
3. +5V power supply (also available for =3.0V)
4. 1/16 duty cycle
5. Easy interface with 4-bit or 8-bit MPU
6. BKL to be driven by pin1, pin2, or pin15, pin16 or A, K
7. 40x2 characters

## Outline dimension



Unit: mm

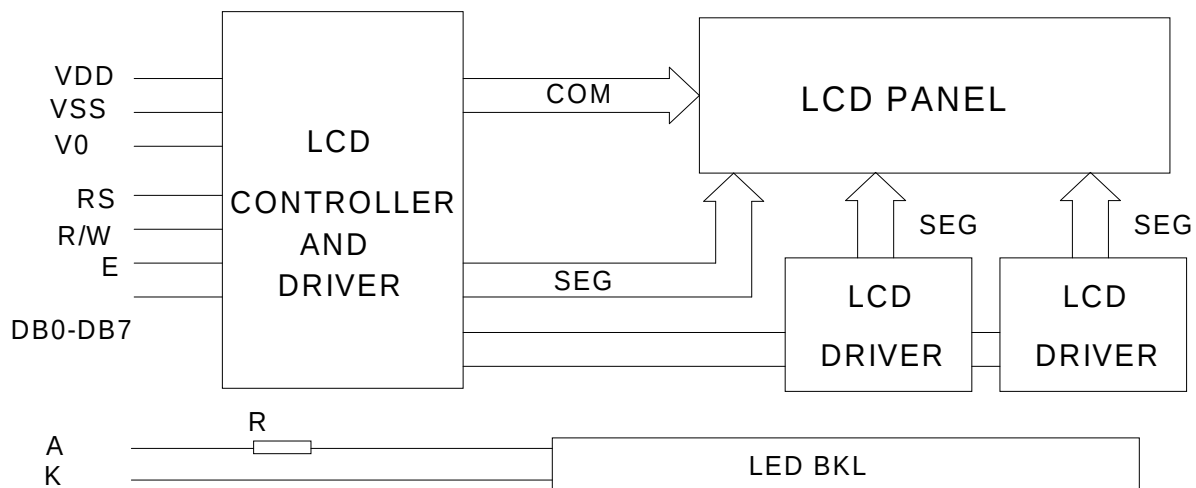
## Absolute maximum ratings

| Item                        | Symbol          | Standard |   |              | Unit               |
|-----------------------------|-----------------|----------|---|--------------|--------------------|
| Power voltage               | $V_{DD}-V_{SS}$ | -0.3     | - | 7.0          | V                  |
| Input voltage               | $V_{IN}$        | -0.3     | - | $V_{DD}+0.3$ |                    |
| Operating temperature range | Top             | 0        | - | +50          | $^{\circ}\text{C}$ |
| Storage temperature range   | Tst             | -10      | - | +60          |                    |

\*Wide temperature range is available

(operating/storage temperature as  $-20\sim+70/-30\sim+80^{\circ}\text{C}$ )

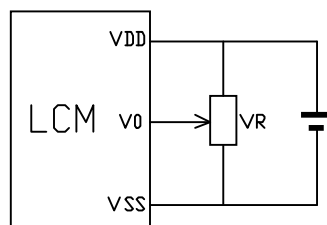
## Block diagram



## Interface pin description

| Pin no. | Symbol          | External connection  | Function                                                                                                                                                      |
|---------|-----------------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | V <sub>SS</sub> | Power supply         | Signal ground for LCM (GND)                                                                                                                                   |
| 2       | V <sub>DD</sub> |                      | Power supply for logic for LCM                                                                                                                                |
| 3       | V <sub>0</sub>  |                      | Contrast adjust                                                                                                                                               |
| 4       | RS              | MPU                  | Register select signal                                                                                                                                        |
| 5       | R/W             | MPU                  | Read/write select signal                                                                                                                                      |
| 6       | E               | MPU                  | Operation (data read/write) enable signal                                                                                                                     |
| 7~10    | DB0~DB3         | MPU                  | Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation. |
| 11~14   | DB4~DB7         | MPU                  | Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU                                                             |
| 15      | A               | LED BKL power supply | Power supply for BKL (Anode)                                                                                                                                  |
| 16      | K               |                      | Power supply for BKL (GND)                                                                                                                                    |

## Contrast adjust



V<sub>DD</sub>-V<sub>0</sub>: LCD Driving voltage

VR: 10k~20k

## Optical characteristics

STN type display module (Ta=25 °C, VDD=5.0V)

| Item                 | Symbol   | Condition    | Min. | Typ. | Max. | Unit |
|----------------------|----------|--------------|------|------|------|------|
| Viewing angle        | $\theta$ | $C_r \geq 2$ | -60  | -    | 35   | deg  |
|                      | $\Phi$   |              | -40  | -    | 40   |      |
| Contrast ratio       | $C_r$    |              | -    | 8    | -    | -    |
| Response time (rise) | $T_r$    | -            | -    | 200  | 250  | ms   |
| Response time (fall) | $T_r$    | -            | -    | 300  | 350  |      |

## Electrical characteristics

DC characteristics

| Parameter                | Symbol       | Conditions                  | Min. | Typ. | Max.     | Unit |
|--------------------------|--------------|-----------------------------|------|------|----------|------|
| Supply voltage for LCD   | $V_{DD}-V_0$ | Ta =25 °C                   | -    | 4.5  | -        | V    |
| Input voltage            | $V_{DD}$     |                             | 4.7  | 5.0  | 5.5      |      |
| Supply current           | $I_{DD}$     | Ta=25 °C, VDD=5.0V          | -    | 1    | 2.5      | mA   |
| Input leakage current    | $I_{LKG}$    |                             | -    | -    | 1.0      | uA   |
| “H” level input voltage  | $V_{IH}$     |                             | 2.2  | -    | $V_{DD}$ | V    |
| “L” level input voltage  | $V_{IL}$     | Twice initial value or less | 0    | -    | 0.6      |      |
| “H” level output voltage | $V_{OH}$     | LOH=-0.25mA                 | 2.4  | -    | -        |      |
| “L” level output voltage | $V_{OL}$     | LOH=1.6mA                   | -    | -    | 0.4      |      |
| Backlight supply voltage | $V_F$        |                             | -    | -    | -        |      |

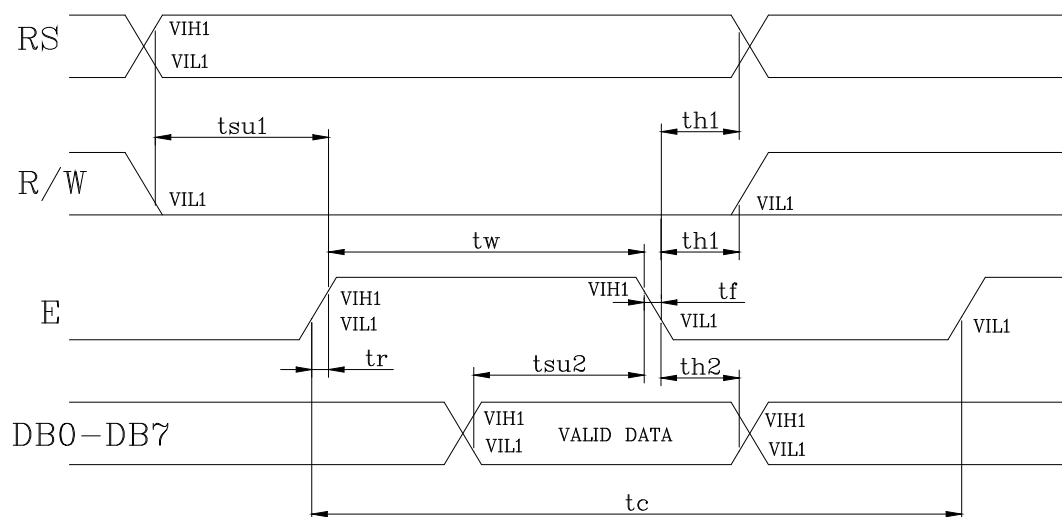
**Read cycle** (Ta=25 °C, VDD=5.0V)

| Parameter                 | Symbol     | Test pin | Min. | Typ. | Max. | Unit |
|---------------------------|------------|----------|------|------|------|------|
| Enable cycle time         | $t_c$      | E        | 500  | -    | -    | ns   |
| Enable pulse width        | $t_w$      |          | 230  | -    | -    |      |
| Enable rise/fall time     | $t_r, t_f$ |          | -    | -    | 20   |      |
| RS; R/W setup time        | $t_{su}$   | RS; R/W  | 40   | -    | -    |      |
| RS; R/W address hold time | $t_h$      |          | 10   | -    | -    |      |
| Data output delay         | $t_d$      | DB0~DB7  | -    | -    | 120  |      |
| Data hold time            | $t_{dh}$   |          | 5    | -    | -    |      |

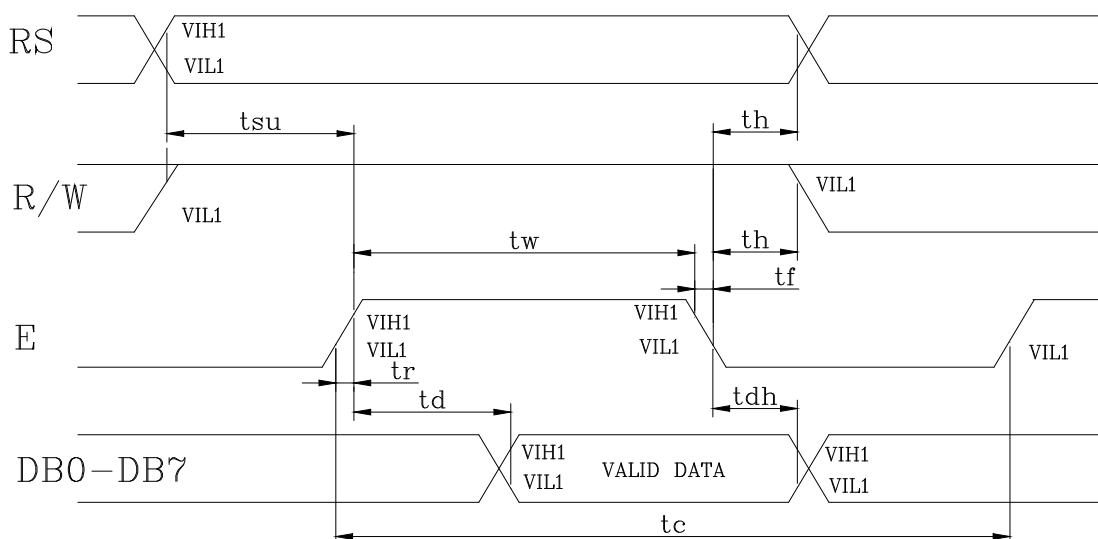
**Write cycle** (Ta=25 °C, VDD=5.0V)

| Parameter                 | Symbol     | Test pin | Min. | Typ. | Max. | Unit |
|---------------------------|------------|----------|------|------|------|------|
| Enable cycle time         | $t_c$      | E        | 500  | -    | -    | ns   |
| Enable pulse width        | $t_w$      |          | 230  | -    | -    |      |
| Enable rise/fall time     | $t_r, t_f$ |          | -    | -    | 20   |      |
| RS; R/W setup time        | $t_{su1}$  | RS; R/W  | 40   | -    | -    |      |
| RS; R/W address hold time | $t_{h1}$   |          | 10   | -    | -    |      |
| Data output delay         | $t_{su2}$  | DB0~DB7  | 80   | -    | -    |      |
| Data hold time            | $t_{h2}$   |          | 10   | -    | -    |      |

## Write mode timing diagram



## Read mode timing diagram



## Instruction description

### Outline

To overcome the speed difference between the internal clock of S6A0069 and the MPU clock, S6A0069 performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).

Instructions can be divided largely into four groups:

- 1) S6A0069U function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read "High". Busy flag check must be preceded by the next instruction. When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/ 2 fuss for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "LOW".

## Contents

### 1) Clear display

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   |

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, brings the cursor to the left edge on the first line of the display. Make the entry mode increment (I/D="High").

### 2) Return home

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | -   |

Return home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

### 3) Entry mode set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | SH  |

Set the moving direction of cursor and display.

### I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D="high", cursor/blink moves to right and DDRAM address is increased by 1.

When I/D="Low", cursor/blink moves to left and DDRAM address is increased by 1.

\*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

(I/D="high". shift left, I/D="Low". Shift right).

### SH: Shift of entire display

When DDRAM read (CGRAM read/write) operation or SH="Low", shifting of entire display is not performed..

If SH="High" and DDRAM write operation, shift of entire display is performed according to I/D value.

(I/D="High". Shift left, I/D="Low". Shift right).

### 4) Display ON/OFF control

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   |

Control display/cursor/blink ON/OFF 1 bit register.

**D: Display ON/OFF control bit**

When D="High", entire display is turned on.

When D="Low", display is turned off, but display data remains in DDRAM.

**C: cursor ON/OFF control bit**

When D="High", cursor is turned on.

When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

**B: Cursor blink ON/OFF control bit**

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.

When B="Low", blink is off.

## 5) Cursor or display shift

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 0   | 1   | S/C | R/L | -   | -   |

Shifting of right/left cursor position or display without writing or reading of display data. This instruction is used to correct or search display data. (Refer to Table 6) During 2-line mode display, cursor moves to the 2<sup>nd</sup> line after the 40<sup>th</sup> digit of the 1<sup>st</sup> line. When display data is shifted repeatedly, each line is shifted individually. When display shift is performed, the contents of the address counter are not changed.

**Shift patterns according to S/C and R/L bits**

| S/C | R/L | Operation                                                                 |
|-----|-----|---------------------------------------------------------------------------|
| 0   | 0   | Shift cursor to the left, AC is decreased by 1                            |
| 0   | 1   | Shift cursor to the right, AC is increased by 1                           |
| 1   | 0   | Shift all the display to the left, cursor moves according to the display  |
| 1   | 1   | Shift all the display to the right, cursor moves according to the display |

## 6) Function set

| RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0   | 0   | 0   | 1   | DL  | N   | F   | -   | -   |

**DL: Interface data length control bit**

When DL="High", it means 8-bit bus mode with MPU.

When DL="Low", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

**N: Display line number control bit**

When N="Low", 1-line display mode is set.

When N="High", 2-line display mode is set.

**F: Display line number control bit**

When F="Low", 5x8 dots format display mode is set.

When F="High", 5x11 dots format display mode.

## 7) Set CGRAM address

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

## 8) Set DDRAM address

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 0  | 1   | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU. When 1-line display mode (N=LOW), DDRAM address is from "00H" to "4FH". In 2-line display mode (N=High), DDRAM address in the 1<sup>st</sup> line is from "00H" to "27H", and DDRAM address in the 2<sup>nd</sup> line is from "40H" to "67H".

## 9) Read busy flag &amp; address

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0  | 1  | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 |

This instruction shows whether S6A0069U is in internal operation or not. If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then if the next instruction can be performed. In this instruction you can also read the value of the address counter.

## 10) Write data to RAM

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 0  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

## 11) Read data from RAM

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 1  | 1  | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  |

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction. It also transfers RAM data to output data register. After read operation, address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

**NOTE:** In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates next address position, but only the previous data can be read by the read instruction.



## Instruction table

| Instruction                | Instruction code |     |     |     |     |     |     |     |     |     | Description                                                                                                                      | Execution Time<br>(fosc= 270 KHZ) |
|----------------------------|------------------|-----|-----|-----|-----|-----|-----|-----|-----|-----|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------|
|                            | RS               | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |                                                                                                                                  |                                   |
| Clear Display              | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | Write "20H" to DDRA and set DDRAM address to "00H" from AC                                                                       | 1.53ms                            |
| Return Home                | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 0   | 1   | -   | Set DDRAM address to "00H" From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed. | 1.53ms                            |
| Entry mode Set             | 0                | 0   | 0   | 0   | 0   | 0   | 0   | 1   | I/D | SH  | Assign cursor moving direction And blinking of entire display                                                                    | 39us                              |
| Display ON/ OFF control    | 0                | 0   | 0   | 0   | 0   | 0   | 1   | D   | C   | B   | Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.                                                      |                                   |
| Cursor or Display shift    | 0                | 0   | 0   | 0   | 0   | 1   | S/C | R/L | -   | -   | Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.                              | 39us                              |
| Function set               | 0                | 0   | 0   | 0   | 1   | DL  | N   | F   | -   | -   | Set interface data length (DL: 8-Bit/4-bit), numbers of displayLine (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)     | 39us                              |
| Set CGRAM Address          | 0                | 0   | 0   | 1   | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set CGRAM address in addressCounter.                                                                                             | 39us                              |
| Set DDRAM Address          | 0                | 0   | 1   | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set DDRAM address in addressCounter.                                                                                             | 39us                              |
| Read busy Flag and Address | 0                | 1   | BF  | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Whether during internal Operation or not can be knownBy reading BF. The contents of Address counter can also be read.            | 0us                               |
| Write data to Address      | 1                | 0   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Write data into internal RAM (DDRAM/CGRAM).                                                                                      | 43us                              |
| Read data From RAM         | 1                | 1   | D7  | D6  | D5  | D4  | D3  | D2  | D1  | D0  | Read data from internal RAM (DDRAM/CGRAM).                                                                                       | 43us                              |

NOTE: When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

DDRAM address:

|    |    |    |    |    |    |    |    | Display position |    |    |    |    |    |    |    |  |  |  |  |
|----|----|----|----|----|----|----|----|------------------|----|----|----|----|----|----|----|--|--|--|--|
| 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | -----            | 34 | 35 | 36 | 37 | 38 | 39 | 40 |  |  |  |  |
| 00 | 01 | 02 | 03 | 04 | 05 | 06 | 07 | -----            | 21 | 22 | 23 | 24 | 25 | 26 | 27 |  |  |  |  |
| 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | -----            | 61 | 62 | 63 | 64 | 65 | 66 | 67 |  |  |  |  |

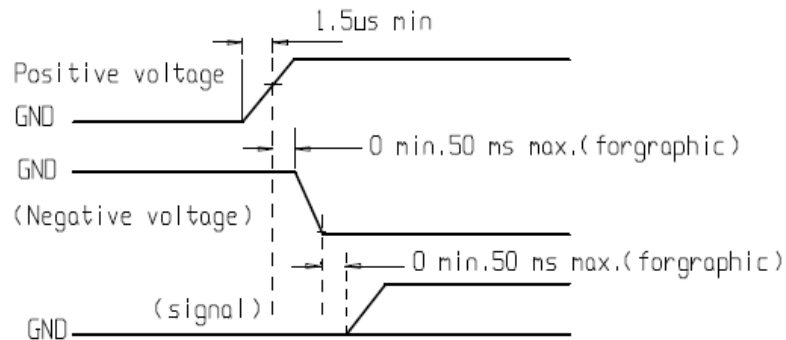
DDRAM address

## Standard character pattern

| Upper<br>4bit<br>Lower<br>4bit |                  | LLLL | LLLH | LLHL | LLHH | LHLL | LHLH | LHHL | LHHH | HLLL | HLLH | HLHL | HLHH | HHLL | HHLH | HHHL | HHHH |
|--------------------------------|------------------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| LLLL                           | CG<br>RAM<br>(1) |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LLLH                           | (2)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LLHL                           | (3)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LLHH                           | (4)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LHLL                           | (5)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LHLH                           | (6)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LHHL                           | (7)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| LHHH                           | (8)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HLLL                           | (1)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HLLH                           | (2)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HLHL                           | (3)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HLHH                           | (4)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HHLL                           | (5)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HHLH                           | (6)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HHHL                           | (7)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |
| HHHH                           | (8)              |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

## LCM Operation Precautions

- (1) It is an indispensable condition to drive LCD within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current driver should be avoided.
- (2) Response time will be extremely delayed at lower temperature than the specified operating temperature range and on the other hand LCD's show dark blue color in the higher temperature. However, those phenomena do not mean any malfunction or display out of order with LCD's, which will come back in the specified operation temperature range.
- (3) If the display area is pushed hard during operation, some fonts will be abnormally displayed. But it resumes normal condition after turning off once.
- (4) A slight dew depositing on terminals could be a cause for electrochemical reaction resulting in terminal open circuit.
- (5) Display contrast varies with the change of liquid crystal driving voltage ( $V_o$ ). Adjust  $V_o$  to show the best contrast.
- (6) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it is suggested to use the LCD under the relative condition of 40°C, 85% RH.
- (7) When turning the power on, input each signal after the positive/negative voltage becomes stable.



- (8) The backlight must be operated within the condition of specification. The overload current or too high voltage will reduce the life time or destroy the backlight.

## Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Please handle the polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
  - Isopropyl alcohol

- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water

- Ketone

- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the IO cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.

- Tools required for assembling, such as soldering irons, must be properly grounded.

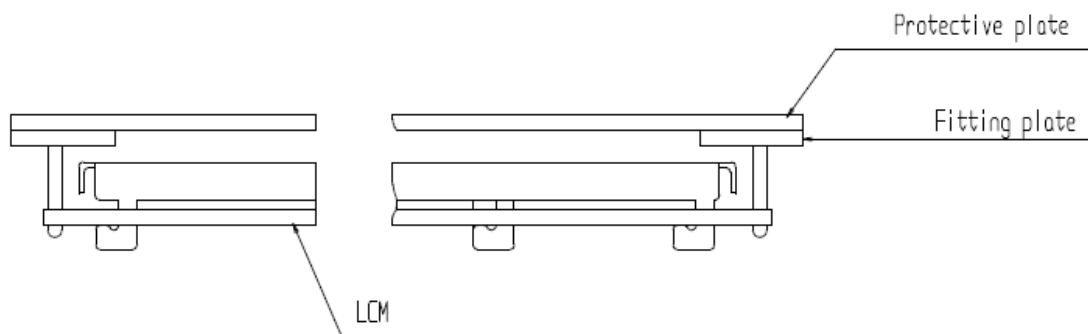
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

### Installing Precautions

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.

### Storage Precautions

In case of storing for a long period of time for the purpose of replacement use, the following ways are recommended.

- (1) Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it, and with no desiccant.
- (2) Placing in a dark place where neither exposure to direct sunlight nor light is, keeping temperature in the range from -30°C to 80°C
- (3) Storing with no touch on polarizer surface by anything else. (It is recommended to store them as they have been contained in the inner container at the time of delivery from us.)

### Safety

- (1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.
- (2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

### Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature. If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability. To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity

etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.