A M O T E C

ADM12864G

SPECIFICATIONS OF LCD MODULE

ADM12864G is a dot matrix graphic LCD module, which is fabricated by low power COMS technology. It can display 128*64 dots size LCD panel using a 128*64 bit-mapped Display Data RAM (DDRAM). It interfaces with an 8-bit microprocessor.

1.Features

- Display format: 128*64 dots matrix graphic
- Easy interface with 8-bit MPU
- Low power consumption
- LED back-light
- Driving method: 1/64 duty, 1/6.7 bias
- LCD driver IC: KS0108B、KS0107B
- Connector: Zebra

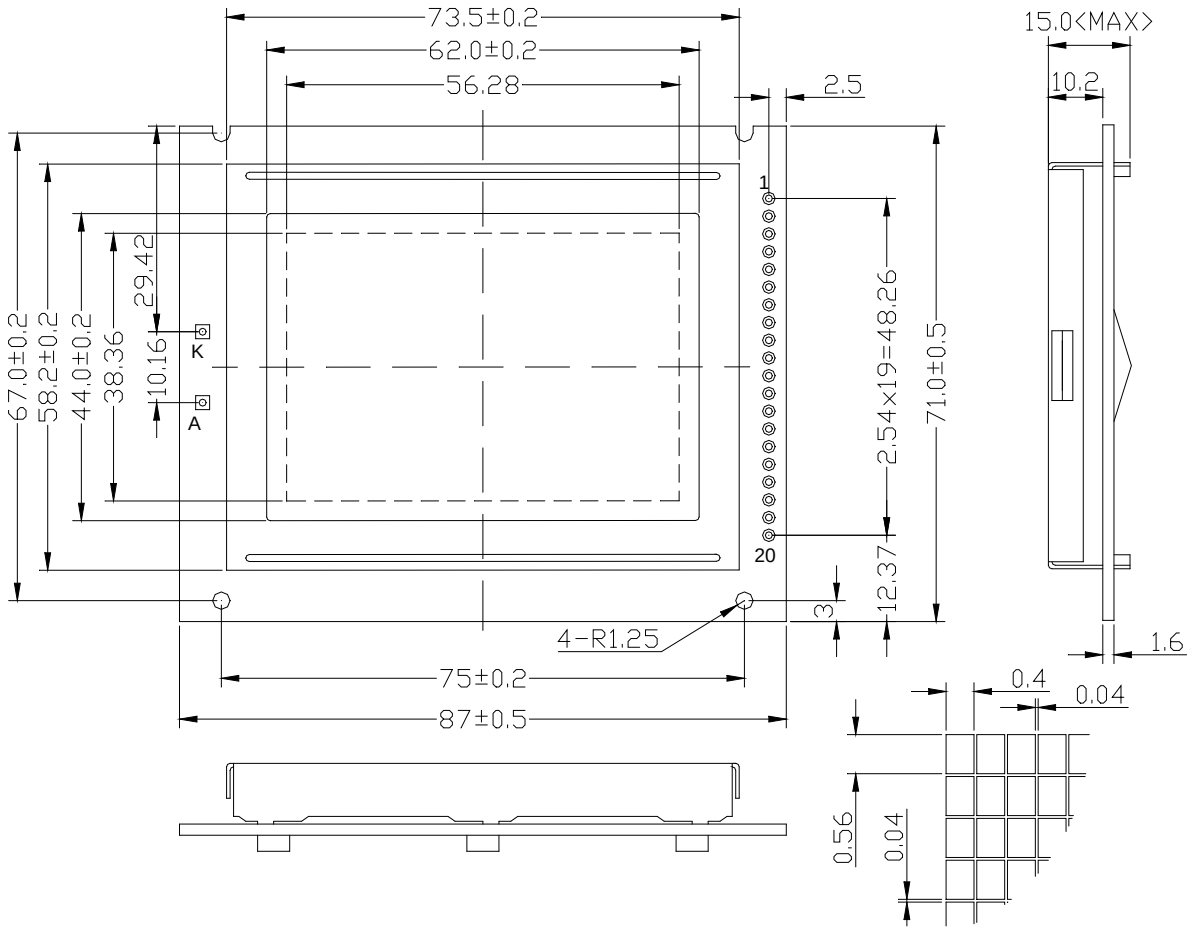
2.Mechanical Specifications

Item	Dimension	Unit
Viewing Area (W*H)	62.0*44.0	mm
Number of Dots	128.0*64.0	PCS
Dot Size (W*H)	0.40*0.56	mm
Dot Pitch (W*H)	0.44*0.60	mm
Module Size With B/L	93.0*70.0*15.0	mm

3. Absolute Maximum Ratings

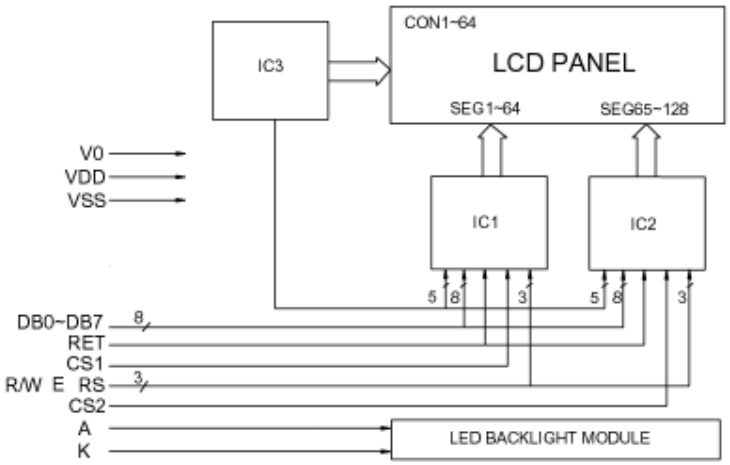
Item	Symbol	Min	Max	Unit
Power Voltage	V_{DD} -V_{SS}	0	5.5	V
Input Voltage	V_I	V_{SS}	V_{DD}	
Operating Temperature Range	V_{OP}	0	+50	℃
Storage Temperature Range	T_{ST}	-10	+60	

4.Mechanical diagram



PIN	1	2	3	4	5	6	7	8	9	10
SIGNAL	VSS	VDD	V0	RS	R/W	E	DB0	DB1	DB2	DB3
PIN	11	12	13	14	15	16	17	18	19	20
SIGNAL	DB4	DB5	DB6	DB7	CS1	RST	VEE	CS2	NC	NC

5.Block diagram



6.Description Of Terminals

Pin No.	Pin Name	Input/ Output	Function
1	VSS	—	VSS: GND
2	VDD	—	VDD: +5V
3	V0	—	Adjustable resistor terminal With VEE pin to adjust LCD contrast.
4	RS	Input	Register selection **RS** **Description** H The data in DB [7:0] is disp lay data. L The data in DB [7:0] is control data
5	R/W	Input	Read or Write **RW** **Description** H Data appears at DB[7:0] and can be read by the CPU L Display data DB[7:0] can be written at falling edge of E
6	E	Input	Enable signal **E** **Description** H Read data in DB[7:0] appears while E= “High”. L Display data DB[7:0] is latched at falling edge of E.
7~14	DB0~7	I/o	Data bus [0~7] Bi-directional data bus
15	CS1	Input	Chip selection When CS1=H, CS2=L, select IC1
16	RST	Input	Reset signal. When RSTB=L 1. ON/OFF register becomes set by 0.(display off) 2. Display start line register becomes set by 0 (Z -address 0 set, display from line 0) After releasing reset, this condition can be changed only by Instruction.
17	VEE	NC	
18	CS2	Input	Chip selection When CS1=L, CS2=H, select IC2
19~20	NC	—	—

7.Optical Characteristics

➢ **STN type display module (Ta=25℃, VDD=5.0V)**

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geqslant 2$	-60	-	35	Deg
	Φ		-40	-	40	
Contrast ratio	C_r		-	6	-	-
Response time (rise)	T_r	-	-	150	250	ms
Response time (fall)	T_r	-	-	150	250	

8. Electrical Characteristics

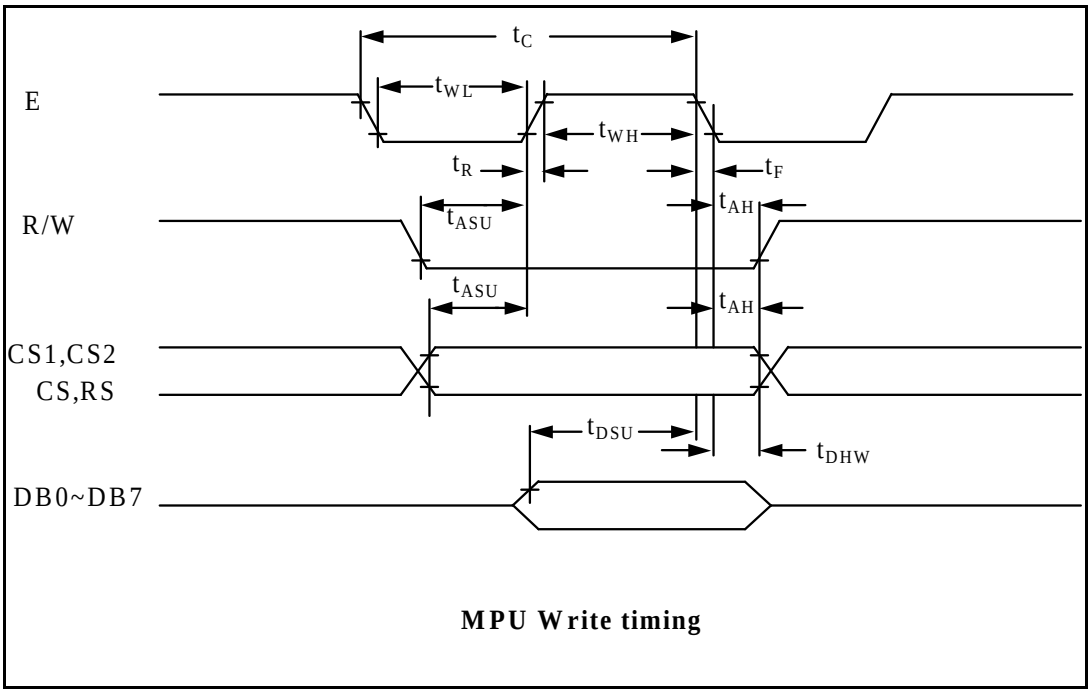
➢ DC Characteristics

Parameter	Symbol	Conditions	Min.	Type	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_O$	T_A=25℃	—	14	—	V
Input voltage	V_{DD}		4.7	—	5.5	V
Supply current	I_{DD}	V_{DD}=5.0V;T_A=25℃	—	3.5	5.0	mA
Input leakage current	I_{LKG}		—	—	1.0	μA
“H” level input voltage	V_{IH}		2.2	—	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	—	0.6	V
“H” level output voltage	V_{OH}	L_{OH}= -0.25mA	2.4	—	—	V
“L” level output voltage	V_{OL}	L_{OL}=1.6mA	—	—	0.4	V
Backlight supply voltage	V_F		—	4.2	4.5	V

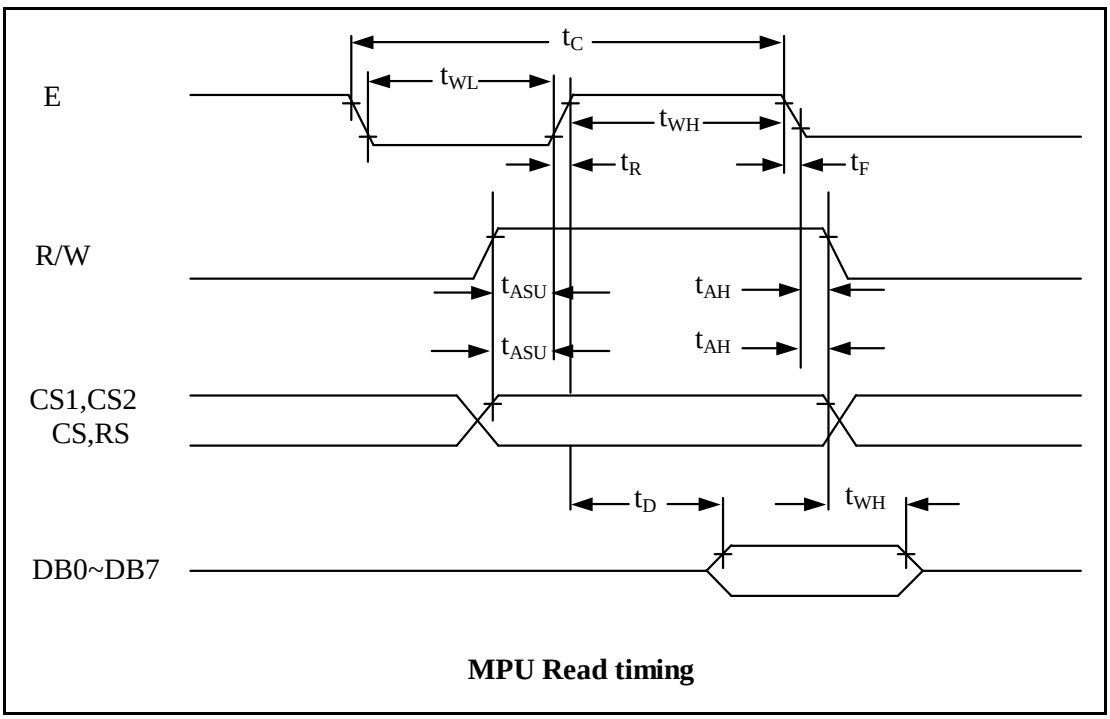
➢ AC. Characteristics

VDD=5V, Ta=25℃

Characteristic	Symbol	Min	Typ	Max	Units
E Cycle	t_C	1000	-	-	ns
E High Level Width	t_{WH}	450	-	-	
E Low Level Width	t_{WL}	450	-	-	
E Rise Time	t_R	-	-	25	
E Fall Time	t_F	-	-	25	
Address Set-Up Time	t_{ASU}	140	-	-	
Address Hold Time	t_{AH}	10	-	-	
Data Set-Up Time	t_{SU}	200	-	-	
Data Delay Time	t_D	-	-	320	
Data Hold Time (Write)	t_{DHW}	10	-	-	
Data Hold Time (Read)	t_{DHR}	20	-	-	



MPU Write timing



MPU Read timing

9.OPERATING PRINCIPLES & METHODS

➢ I/O Buffer

Input buffer controls the status between the enable and disable of chip. Unless the CS1B to CS3 is in active mode, Input or output of data and instruction does not execute. Therefore internal state is not change. But RSTB and ADC can operate regardless CS!B -CS3.

➢ Input register

Input register is provided to interface with MPU which is different operating frequency. Input register stores the data temporarily before writing it into display RAM.
When CS1B to CS3 are in the active mode, R/W and RS select the input register. The data from MPU is written into input register. Then writing it into display RAM. Data latched for falling of the E signal and write automatically into the display data RAM by internal operation.

➢ Output register

Output register stores the data temporarily from display data RAM when CS1B, CS2B and CS3 are in active mode and R/W and RS=H, stored data in display data RAM is latched in output register. When CS1B to CS3 is in active mode and R/W=H , RS=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data, which is latched. That is to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

RS	R/W	Function
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

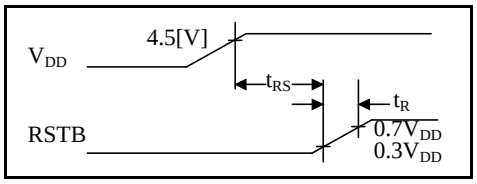
➢ Reset

The system can be initialized by setting RSTB terminal at low level when turning power on, receiving instruction from MPU. When RSTB becomes low, following procedure is occurred.
1. Display off
2. Display start line register become set by 0.(Z-address 0)

While RSTB is low, No instruction except status read can by accepted. Therefore, execute other instructions after making sure that DB4= (clear RSTB) and DB7=0 (ready) by status read instruction.
The conditions of power supply at initial power up are shown in table 1.

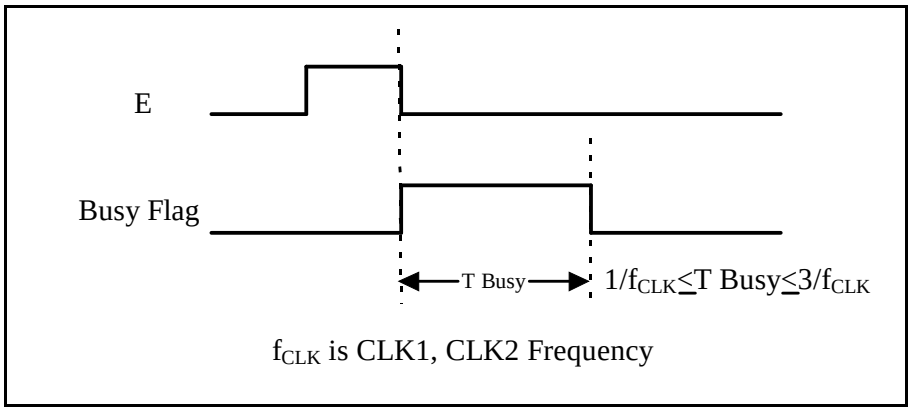
Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	-	-	us
Rise Time	t_R	-	-	200	ns



➢ Busy flag

Busy flag indicates that KS0108B is operating or no operating. When busy flag is high, KS0108B is in internal operating.
When busy flag is low, KS0108B can accept the data or instruction.
DB7indicates busy flag of the KS0108B.



➢ Display On/Off Flip-Flop

The display on/off flip-flop makes on/off the liquid crystal display. When flip -flop is reset (logical low), selective voltage or non-selective voltage appears on segment output terminals. When flip-flop is set (logic high), non selective voltage appears on segment output terminals regardless of display RAM data.

The display on/off flip-flop can changes status by instruction. The display data at all segments disappear while RSTB is low.
The status of the flip-flop is output to DB5 by status read instruction.
The display on/off flip-flop synchronized by CL signal.

➢ X Page Register

X page register designates pages of the internal display data RAM.
Count function is not available. An address is set by instruction.

➢ Y address counter

Y address counter designates address of the internal display data RAM. An address is set by instruction and is increased by 1 automatically by r ead or write operations of display data.

➢ Display Data RAM

Display data RAM stores a display data for liquid crystal display. To indicate on state dot matrix of liquid crystal display, write datra1. The other way, off state, writes 0.
Display data RAM addre ss and segment output can be controlled by ADC signal.
ADC=H => Y-address 0: S1~Y address 63: S64
ADC=L => Y-address 0: S64~Yaddress 63: S1

ADC terminal connect the V_{DD} or V_{SS}.

- **Display Start Line Register**

  The display start line register indicates of displa y data RAM to display top line of liquid crystal display. Bit data (DB<0.5>) of the display start line set instruction is latched in display start line register. Latched data is transferred to the Z address counter while FRM is high, presetting the Z addre ss counter. It is used for scrolling of the liquid crystal display screen.

10.Display Control Instruction

The display control instructions control the internal state of the KS0108B. Instruction is received from MPU to KS0108B for the display control. The f ollowing table shows various instructions.

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Function
Read Display Date	1	1	Read data								Reads data (DB[7:0]) from display data RAM to the data bus.
Write Display Date	1	0	Write data								Writes data (DB[7:0]) into the DDRAM. After writing instruction, Y address is incriminated by 1 automatically
Status Read	0	1	Bus y	0	ON /OF F	Re- set	0	0	0	0	Reads the internal status BUSY 0: Ready 1: In operation ON/OFF 0: Display ON 1: Display OFF RESET 0: Normal 1: Reset
Set Address (Y address)	0	0	0	1	Y address (0~63)						Sets the Y address at the column address counter
Set Display Start Line	0	0	1	1	Display start line (0~63)						Indicates the Display Data RAM displayed at the top of the screen.
Set Address (X address)	0	0	1	0	1	1	1	Page (0~7)			Sets the X address at the X address register.
Display On/off	0	0	0	0	1	1	1	1	1	0/1	Controls the display ON or OFF. The internal status and the DDRAM data is not affected. 0: OFF, 1: ON

➢ Display On/Off

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

The display data appears when D is 1 and disappears when D is 0.
Though the data is not on the screen with D=0, it remains in the display data RAM.
Therefore, you can make it appear by changing D=0 into D=1.

➢ Set Address (Y Address)

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Y address (AC0~AC5) of the display data RAM is set in the Y address counter.
An address is set by instruction and increased by 1 automatically by read or write operations of display data.

➢ Set Page (X Address)

X address (AC0~AC2) of the display data RAM is set in the X address register.
Writing or reading to or from MPU is executed in this specified page until the next page is set.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	AC2	AC1	AC0

➢ Display Start Line (Z Address)

Z address (AC0~AC5) of the display data RAM is set in the display start line register and displayed at the top of the screen.
When the display duty cycle is 1/64 or others (1/32~1/64), the data of total line number o f LCD screen, from the line specified by display start line instruction, is displayed.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	AC5	AC4	AC3	AC2	AC1	AC0

➢ Status Read

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

- BUSY
  When BUSY is 1, the Chip is executing internal operation and no instructions are accepted.
  When BUSY is 0, the Chip is ready to accept any instructions.
- ON/OFF
  When ON/OFF is 1, the display is on.
  When ON/OFF is 0, the display is off.
- RESET
  When RESET is 1, the system is being initialized.
  In this condition, no instructions except status read can be accepted.

When RESET is 0, initializing has finished and the system is in the usual operation condition.

➢ Write Display Data

Writes data (D0~D7) into the display data RAM.
After writing instruction, Y address is increased by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

➢ Read Display Data

Reads data (D0~D7) from the display data RAM.
After reading instruction, Y address is increas ed by 1 automatically.

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0