

AMOTEC

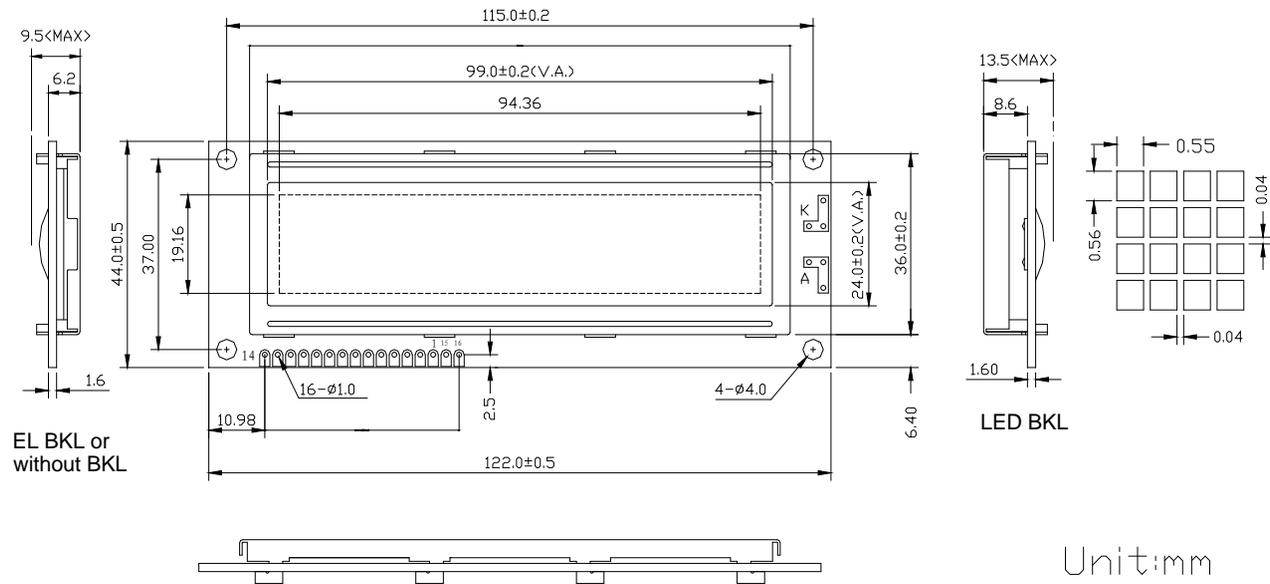
ADM16032B

SPECIFICATIONS OF LCD MODULE

Features

- 1、 160x32 dots with 8192 chinese character fonts (16x16)
- 2、 128 alpha-numerical fonts (16x8)
- 3、 64x256 bit graphic display RAM
- 4、 Strong display control functions:
Vertical scroll, horizontal bit scroll, line reverse etc
- 5、 +2.7V~+5.5V power supply
- 6、 1/32 duty
- 7、 building boost circuit
- 8、 4 bit, 8 bit, serial interface
- 9、 LED backlight optional

Outline dimension



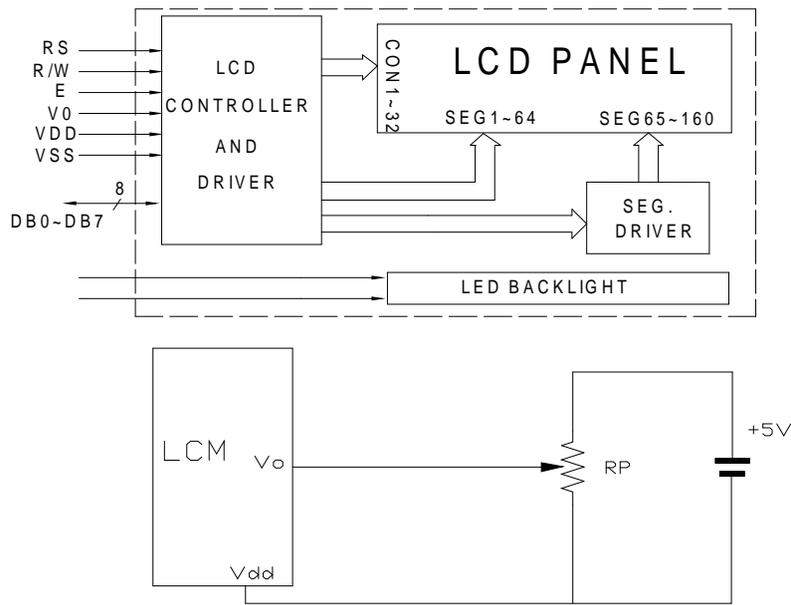
Unit:mm

Absolute maximum ratings

Item	Symbol	Standard	Unit
Power supply voltage	$V_{DD}-V_{SS}$	-0.3 - 6.0	V
Input voltage	V_{IN}	-0.3 - $V_{DD}+0.3$	
Operating temperature range	Top	0 - +50	°C
Storage temperature range	Tst	-10 - +60	

*Wide temperature range is available
(operating/storage temperature as -20~+70/-30~+80°C)

Block diagram



$V_0 - V_{SS}$: LCD DRIVING VOLTAGE

RP: 10K~20K

Interface pin description

Pin no.	Symbol	External connection	Function
1	V_{SS}	Power supply	Signal ground for LCM (GND)
2	V_{DD}		Power supply for logic for LCM
3	V_0		Contrast adjust
4	RS	MPU	Register select signal
5	R/W	MPU	Read/write select signal
6	E	MPU	Operation (data read/write) enable signal
7~10	DB0~DB3	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
11~14	DB4~DB7	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
15	LED+	LED BKL power supply	Power supply for BKL (Anode)
16	LED-		Power supply for BKL (GND)

Optical characteristics

STN type display module ($T_a=25^\circ\text{C}$, $V_{DD}=5.0\text{V}$)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_i \geq 2$	-60	-	35	deg
	Φ		-40	-	40	
Contrast ratio	C_r		-	8	-	-
Response time (rise)	T_r	-	-	200	250	ms
Response time (fall)	T_f	-	-	300	350	

Electrical characteristics

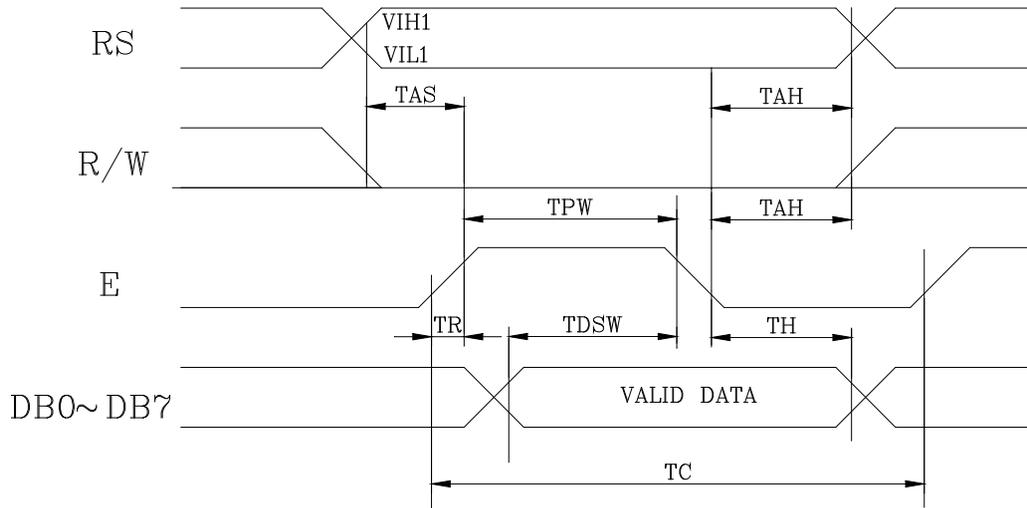
DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	$V_0 - V_{ss}$	$T_a = 25^\circ\text{C}$ $V = +5\text{V}$	-	6.5	-	V
Input voltage	V_{DD}	$V = 3.3\text{V}$	2.7	3.3	5.5	
		$V = 5\text{V}$	4.7	5.0	5.5	
Supply current	I_{DD}	$T_a = 25^\circ\text{C}$; $V_{DD} = 5.0\text{V}$	-	2	4	mA
Input leakage current	I_{LKG}		-	-	1.0	uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	$LOH = -0.25\text{mA}$	2.4	-	-	
“L” level output voltage	V_{OL}	$LOH = 1.6\text{mA}$	-	-	0.4	
Backlight supply voltage	V_F		-	-	-	

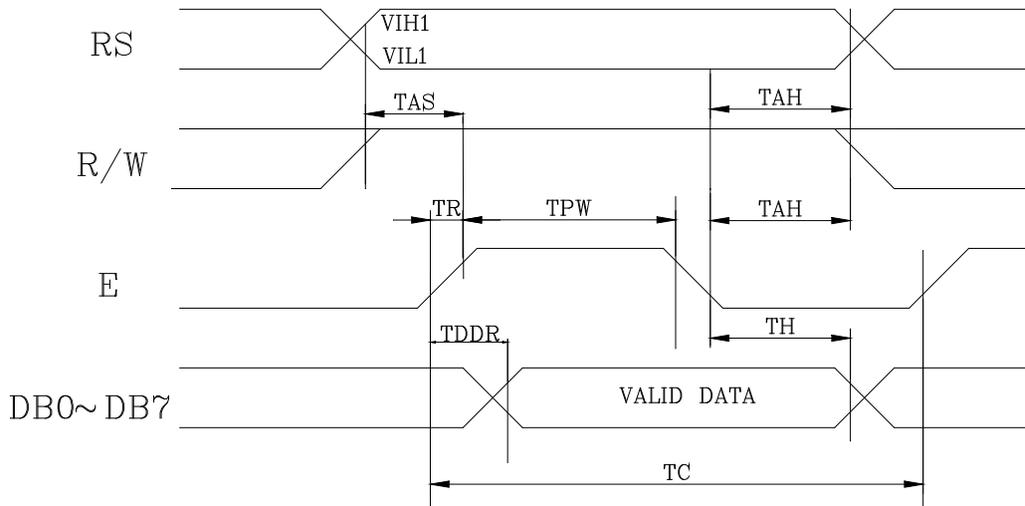
AC Characteristics ($T_A = -30^\circ\text{C} \sim 85^\circ\text{C}$, $V_{DD} = 4.5\text{V}$) Parallel Mode Interface

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<i>Internal Clock Operation</i>						
fOSC	OSC Frequency	$R = 33\text{KW}$	480	540	600	KHz
<i>External Clock Operation</i>						
fEX	External Frequency	-	480	540	600	KHz
	Duty Cycle	-	45	50	55	%
TR,TF	Rise/Fall Time	-	-	-	0.2	μs
<i>Write Mode (Writing data from MPU to ST7920)</i>						
TC	Enable Cycle Time	Pin E	1200	-	-	ns
TPW	Enable Pulse Width	Pin E	140	-	-	ns
TR,TF	Enable Rise/Fall Time	Pin E	-	-	25	ns
TAS	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
TAH	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
TDSW	Data Setup Time	Pins: DB0 - DB7	40	-	-	ns
TH	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns
<i>Read Mode (Reading Data from ST7920 to MPU)</i>						
TC	Enable Cycle Time	Pin E	1200	-	-	ns
TPW	Enable Pulse Width	Pin E	140	-	-	ns
TR,TF	Enable Rise/Fall Time	Pin E	-	-	25	ns
TAS	Address Setup Time	Pins: RS,RW,E	10	-	-	ns
TAH	Address Hold Time	Pins: RS,RW,E	20	-	-	ns
TDDR	Data Delay Time	Pins: DB0 - DB7	-	-	100	ns
TH	Data Hold Time	Pins: DB0 - DB7	20	-	-	ns

Write Timing



Read timing



Function Description

System interface

The ADM16032H supports 3 kinds of bus interface to communicate with MPU: 8-bit parallel, 4-bit parallel and clock synchronized serial interface. Parallel interface is selected by PSB="P" and serial interface is by PSB="S". 8-bit / 4-bit interface is selected by function set instruction DL bit.

Busy Flag (BF)

The LCD module needs a process time for any received instruction. Before finishing the received instruction, any further instruction is not accepted. The process time of each instruction is not equal and the internal process is finished or not can be determined by the BF. Internal operation is in progress while BF="1", that means module is in busy state. No further instructions will be accepted until BF="0". MPU must check BF to determine whether the internal operation is finished or not before issuing instruction.

Character Generation ROM (CGROM) and Half-width Character Generation ROM (HCGROM)

The LCD module is built in a Character Generation ROM (CGROM) to provide 8192 16x16 character fonts and a Half-width Character Generation ROM to provide 128 8x16 alphanumeric characters. It is easy to support multi-language applications such as Chinese and English. Two consecutive bytes are used to specify one 16x16 character or two 8x16 half-width characters. Character codes are written into DDRAM and the corresponding fonts are mapped from CGROM or HCGROM to the display drivers.

Character Generation RAM (CGRAM)

The LCD module is built in a Character Generation RAM (CGRAM) to support user-defined fonts. Four sets of 16x16 bit-mapped RAM spaces are available. These user-defined fonts are displayed the same ways as CGROM fonts by writing the related character code into the DDRAM.

Display Data RAM (DDRAM)

There are 64x256 bytes RAM spaces for the Display Data RAM. It can store display data such as 10 characters (16x16) by 2 lines or 32 characters (8x16) by 4 lines. However, only 2 character-lines (maximum 32 common outputs) can be displayed at one time. Character codes stored in DDRAM will refer to the fonts specified by CGROM, HCGROM and CGRAM. The LCD module can display half-width HCGROM fonts, user-defined CGRAM fonts and full 16x16 CGROM fonts. The character codes in 0000H~0006H will use user-defined fonts in CGRAM. The character codes in 02H~7FH will use half-width alpha numeric fonts. The character code larger than A1H will be treated as 16x16 fonts and will be combined with the next byte automatically. The 16x16 BIG5 fonts are stored in A140H~D75FH while the 16x16 GB fonts are stored in A1A0H~F7FFH. In short:

1. To display HCGROM fonts:

Write 2 bytes of data into DDRAM to display two 8x16 fonts. Each byte represents 1 character. The data is among 02H~7FH.

2. To display CGRAM fonts:

Write 2 bytes of data into DDRAM to display one 16x16 font. Only 0000H, 0002H, 0004H and 0006H are acceptable.

3. To display CGROM fonts:

Write 2 bytes of data into DDRAM to display one 16x16 font. A140H~D75FH are BIG5 code, A1A0H~F7FFH are GB code.

The higher byte (D15~D8) is written first and the lower byte (D7~D0) is the next.

Please refer to Table 1 for the relationship between DDRAM and the address/data of CGRAM.

CGRAM fonts and CGROM fonts can only be displayed in the start position of each address. (Refer to Table 4)

80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
H	L	H	L	H	L	H	L	H	L	H	L	H	L	H	L
S	i	t	r	o	n	i	x	.	.	S	T	7	9	2	0
矽	創	電	子	.	.	中	文	編	碼	(正	確)		
矽	創	電	子	.	.	中	文	編	碼						

Table 4

Incorrect start position

■ Graphic RAM (GDRAM)

Graphic Display RAM has 64x256 bits bit-mapped memory space. GDRAM address is set by writing 2 consecutive bytes of vertical address and horizontal address. Two -byte data (16 bits) configures one GDRAM horizontal address. The Address Counter (AC) will be increased by one automatically after receiving the 16 -bit data for the next operation. After the horizontal address reaching 0FH, the horizontal address will be set to 00H and the vertical address will not change. The procedure is summarized below:

1. Set vertical address (Y) for GDRAM
2. Set horizontal address (X) for GDRAM
3. Write D15~D8 to GDRAM (first byte)
4. Write D7~D0 to GDRAM (second byte)

Please refer to Table 3 for Graphic Display RAM mapping.

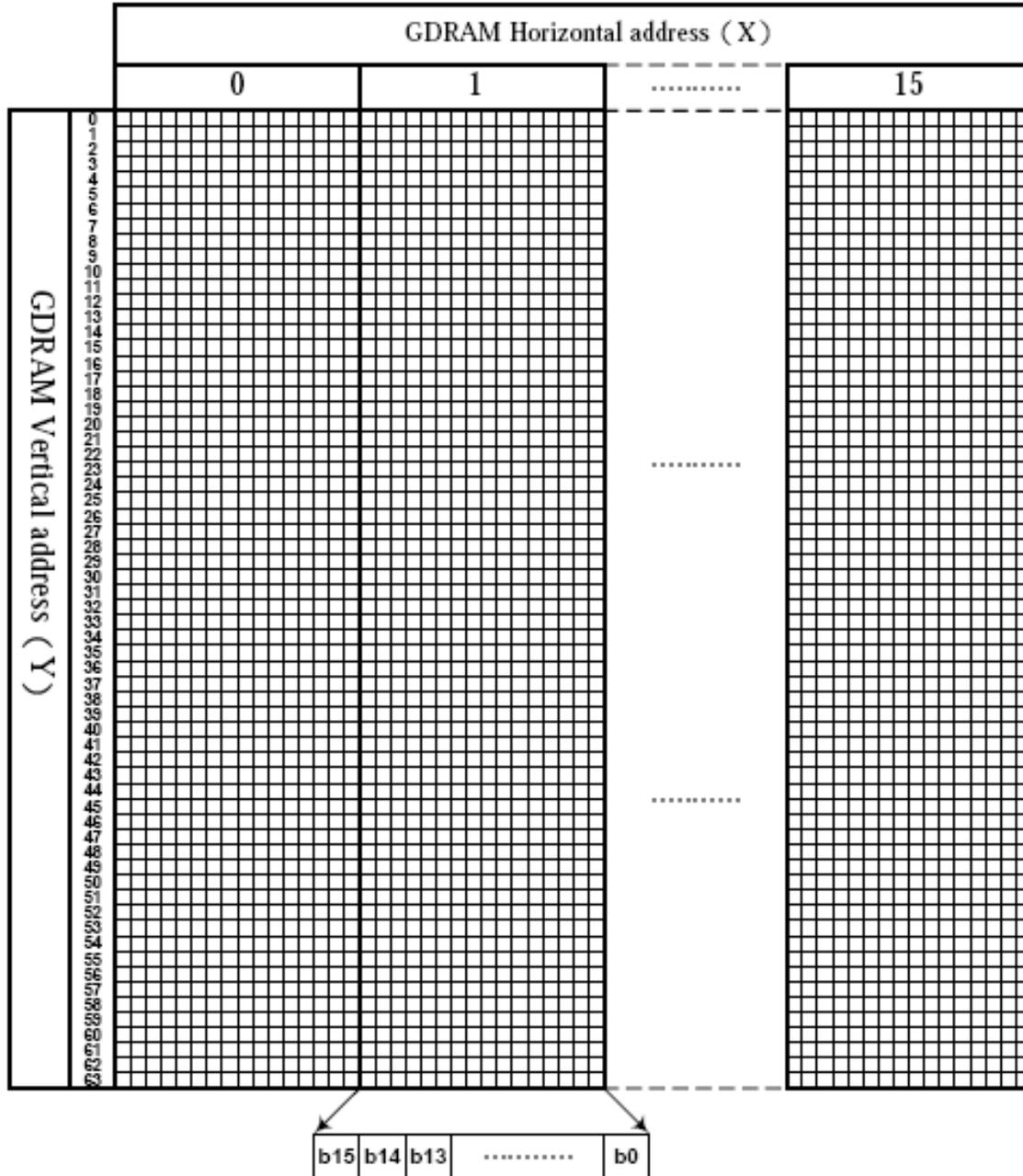


Table 3 GDRAM display coordinates and corresponding address

DDRAM data (char. code)				CGRAM Addr.				CGRAM data (higher byte)								CGRAM data (lower byte)															
B15~ B4	B3	B2	B1	B5	B4	B3	B2	B1	B0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0						
0	X	00	X	00	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0					
					0	0	0	1	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0		
					0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	
					0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	
					0	1	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	
					0	1	0	1	0	0	1	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	
					0	1	1	0	0	1	0	0	1	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	
					1	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0	0	0	0
					1	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
					1	0	1	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
					1	0	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
					1	1	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
					1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
					1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
					0	X	01	X	01	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	1	0
										0	0	0	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0						0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0	
0	0	1	1	0						1	0	1	1	1	0	1	0	1	0	1	0	1	0	0	1	0	0	1	0	0	
0	1	0	0	1						0	0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0	1	0	0	0	
0	1	0	1	0						1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	
0	1	1	0	0						1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	
1	0	0	0	0						1	0	0	0	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	
1	0	0	1	0						1	1	1	1	1	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0
1	0	1	0	0						1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0
1	0	1	1	0						1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	1						0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0
1	1	0	1	0						1	1	1	1	1	1	0	0	0	1	1	1	0	0	1	1	1	0	0	0	0	0
1	1	1	0	1						0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0						0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table1 DDRAM data (character code) vs. CGRAM data/address map

Notes:

1. DDRAM data (character code) bit1 and bit2 are identical with CGRAM address bit4 and bit5.
2. CGRAM address bit0 to bit3 specify total 16 rows. Row -16 is for cursor display. The data in Row -16 will be logically OR to the cursor.
3. CGRAM data for each address is 16 bits.
4. To select the CGRAM font, the bit4 through bit15 of DDRAM data must be "0" while bit0 and bit3 are "don't care".

H/L	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0		☺	☹	♥	♠	♣	♠	•	◐	◑	♂	♀	♩	♪	✳	
1	▶	◀	↑	!!	¶	§	-	‡	↑	↓	→	←	└	↕	▲	▼
2		!	"	#	\$	%	&	'	()	*	+	,	-	.	/
3	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
4	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z	[\]	^	_
6	`	a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z	{		}	~	Δ

16x8 half-width characters

Display command

Instruction Set 1: (RE=0: Basic Instruction)

Inst.	Code											Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Display Clear	0	0	0	0	0	0	0	0	0	0	1	Fill DDRAM with "20H" and set DDRAM address counter (AC) to "00H".	1.6 ms
Return Home	0	0	0	0	0	0	0	0	0	1	X	Set DDRAM address counter (AC) to "00H", and put cursor to origin ; the content of DDRAM are not changed	72 us
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Set cursor position and display shift when doing write or read operation	72 us
Display Control	0	0	0	0	0	0	0	1	D	C	B	D=1: Display ON C=1: Cursor ON B=1: Character Blink ON	72 us
Cursor Display Control	0	0	0	0	0	1	S/C	R/L	X	X	X	Cursor position and display shift control; the content of DDRAM are not changed	72 us
Function Set	0	0	0	0	1	DL	X	0	RE	X	X	DL=1 8-bit interface DL=0 4-bit interface <u>RE=1: extended instruction</u> <u>RE=0: basic instruction</u>	72 us
Set CGRAM Address.	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address to address counter (AC) <u>Make sure that in extended instruction SR=0 (scroll or RAM address select)</u>	72 us
Set DDRAM Address.	0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address to address counter (AC) AC6 is fixed to 0	72 us
Read Busy Flag (BF) & AC.	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Read busy flag (BF) for completion of internal operation, also Read out the value of address counter (AC)	0 us
Write RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data to internal RAM (DDRAM/CGRAM/GDRAM)	72 us
Read RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM/GDRAM)	72 us

ADM16032B

Instruction set 2: (RE=1: extended instruction)

Inst.	Code											Description	Exec time (540KHZ)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Standby	0	0	0	0	0	0	0	0	0	0	1	Enter standby mode, any other instruction can terminate. COM1...32 are halted.	72 us
Scroll or RAM Address. Select	0	0	0	0	0	0	0	0	0	1	SR	SR=1: enable vertical scroll position SR=0: enable CGRAM address (<u>basic instruction</u>)	72 us
Reverse (by line)	0	0	0	0	0	0	0	0	1	R1	R0	Select 1 out of 4 line (in DDRAM) and decide whether to reverse the display by toggling this instruction R1,R0 initial value is 0,0	72 us
Extended Function Set	0	0	0	0	1	DL	X	1	RE	G	0	DL=1 :8-bit interface DL=0 :4-bit interface RE=1: extended instruction set RE=0: basic instruction set G=1 :graphic display ON G=0 :graphic display OFF	72 us
Set Scroll Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		SR=1: AC5~AC0 the address of vertical scroll	72 us
Set Graphic Display RAM Address	0	0	1	0	0	0	AC3	AC2	AC1	AC0	AC0	Set GDRAM address to address counter (AC) Set the vertical address first and followed the horizontal address by consecutive writings Vertical address range: AC5...AC0 Horizontal address range: AC3...AC0	72 us

Note:

1. Make sure that ST7920 is not in busy state by reading the busy flag before sending instruction or data. If using delay loop instead, please make sure the delay time is enough. Please refer to the instruction execution time.
2. "RE" is the selection bit of basic and extended instruction set. After setting the RE bit, the value will be kept. So that the software doesn't have to set RE every time when using the same instruction set.

Initial Setting (Register flag) (RE=0: basic instruction)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Cursor move to right ,DDRAM address counter (AC) plus 1
									1	0	
Display Control	0	0	0	0	0	0	1	D	C	B	Display, cursor and blink are ALL OFF
								0	0	0	
CURSOR DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	X	X	No cursor or display shift operation
							X	X			
FUNCTION SET	0	0	0	0	1	DL	X	0	X	X	8-bit MPU interface , basic instruction set
					1			0			

Initial Setting (Register flag) (RE=1: extended instruction set)

Inst.	Code										Description
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
SCROLL OR RAM ADDR. SELECT	0	0	0	0	0	0	0	0	1	SR	Allow IRAM address or set CGRAM address
										0	
REVERSE	0	0	0	0	0	0	0	1	R1	R0	Begin with normal and toggle to reverse
									0	0	
EXTENDED FUNCTION SET	0	0	0	0	1	DL	X	1	RE	G	Graphic display OFF
									0		

Description of basic instruction set

- Display Clear

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This instruction will change the following items:

1. Fill DDRAM with "20H"(space code).
2. Set DDRAM address counter (AC) to"00H".
3. Set Entry Mode I/D bit to be "1". Cursor moves right and AC adds 1 after write or read operation.

- Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Set address counter (AC) to "00H". Cursor moves to origin. Then content of DDRAM is not changed.

ADM16032B

● Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	S

Set the cursor movement and display shift direction when doing write or read operation.

I/D: Address Counter Control: (Increase/Decrease)

When I/D = "1", cursor moves right, address counter (AC) is increased by 1.

When I/D = "0", cursor moves left, address counter (AC) is decreased by 1.

S: Display Shift Control: (Shift Left/Right)

S	I/D	DESCRIPTION
H	H	Entire display shift left by 1
H	L	Entire display shift right by 1

● Display Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Controls display, cursor and blink ON/OFF.

D: Display ON/OFF control bit

When D = "1", display ON

When D = "0", display OFF, the content of DDRAM is not changed

C: Cursor ON/OFF control bit

When C = "1", cursor ON.

When C = "0", cursor OFF.

B: Character Blink ON/OFF control bit

When B = "1", cursor position blink ON. Then display data (character) in cursor position will blink.

When B = "0", cursor position blink OFF

● Cursor/Display Shift Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

This instruction configures the cursor moving direction or the display shifting direction. The content of DDRAM is not changed.

S/C	R/L	Description	AC Value
L	L	Cursor moves left by 1 position	AC=AC-1
L	H	Cursor moves right by 1 position	AC=AC+1
H	L	Display shift left by 1, cursor also follows to shift.	AC=AC
H	H	Display shift right by 1, cursor also follows to shift.	AC=AC

● Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	-	RE	-	-

DL: 4/8-bit interface control bit

When DL = "1", 8-bit MPU bus interface

When DL = "0", 4-bit MPU bus interface

RE: extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

In same instruction cannot alter DL and RE at once. Make sure that change DL first then RE.

● Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address into address counter (AC)

ADM16032B

AC range is 00H...3FH

Make sure that in extended instruction SR=0 (scroll address or RAM address select)

- **Set DDRAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address into address counter (AC).

First line AC range is 80H...8FH

Second line AC range is 90H...9FH

Third line AC range is A0H...AFH

Fourth line AC range is B0H...BFH

Please note that only 2 lines can be display

- **Read Busy Flag (BF) and Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Read busy flag (BF) can check whether the internal operation is finished or not. At the same time, the value of address counter (AC) is also read. When BF = "1", further instruction(s) will not be accepted until BF = "0".

- **Write Data to RAM**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write data to the internal RAM and increase/decrease the (AC) by 1

Each RAM address (CGRAM, DDRAM and GDRAM...) must write 2 consecutive bytes for 16-bit data. After receiving the second byte, the address counter will increase or decrease by 1 according to the entry mode set control bit.

- **Read RAM Data**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read data from the internal RAM and increase/decrease the (AC) by 1

After the operation mode changed to Read (CGRAM, DDRAM and GDRAM...), a "Dummy Read" is required. There is no need to add a "Dummy Read" for the following bytes unless a new address set instruction is issued.

Description of extended instruction set

- **Standby**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

This Instruction will set ST7920 entering the standby mode. Any other instruction follows this instruction will terminate the standby mode.

The content of DDRAM remains the same.

- **Vertical Scroll or RAM Address Select**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	SR

When SR = "1", the Vertical Scroll mode is enabled.

When SR = "0", "Set CGRAM Address" instruction (**basic instruction**) is enabled.

- **Reverse**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	R1	R0

Select 1 out of 4 lines to reverse the display and to toggle the reverse condition by repeating this instruction.

R1, R0 initial vale is 00. The first time issuing this instruction, the display will be reversed wh ile the second time will return the display become normal.

R1	R0	Description
L	L	First line normal or reverse
L	H	Second line normal or reverse
H	L	Third line normal or reverse
H	H	Fourth line normal or reverse

● **Extended Function Set**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	-	RE	G	-

DL: 4/8-bit interface control bit

When DL = "1", 8-bit MPU interface.

When DL = "0", 4-bit MPU interface.

RE: extended instruction set control bit

When RE = "1", extended instruction set

When RE = "0", basic instruction set

G: Graphic display control bit

When G = "1", Graphic Display ON

When G = "0", Graphic Display OFF

In same instruction cannot alter DL, RE and G at once. Make sure that change DL or G first and then RE.

● **Set Scroll Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

SR=1: AC5~AC0 is vertical scroll displacement address

● **Set Graphic RAM Address**

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	AC5	AC4	AC3	AC2	AC1	AC0

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	0	0	AC3	AC2	AC1	AC0

Set GDRAM address into address counter (AC). This is a 2 -byte instruction.

The first instruction sets the vertical address while the second one sets the horizontal address (write 2 consecutive bytes to complete the vertical and horizontal address setting).

Vertical address range is AC5...AC0

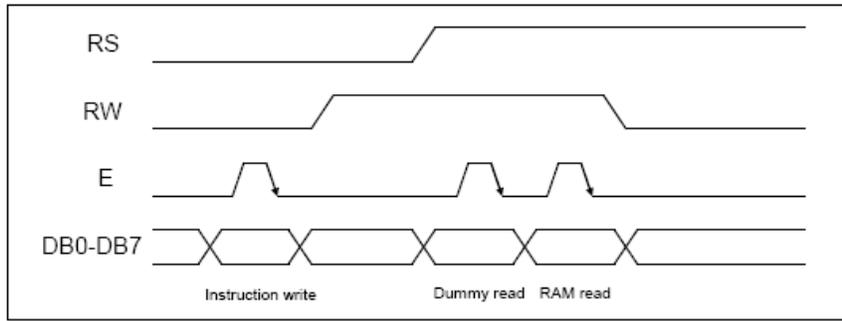
Horizontal address range is AC3...AC0

The address counter (AC) of graphic RAM (GRAM) will be increased automatically after the vertical and horizontal addresses are set. After horizontal address is increased up to 0FH, it will automatically return to 00H. However, the vertical address will not increase as the result of the same action.

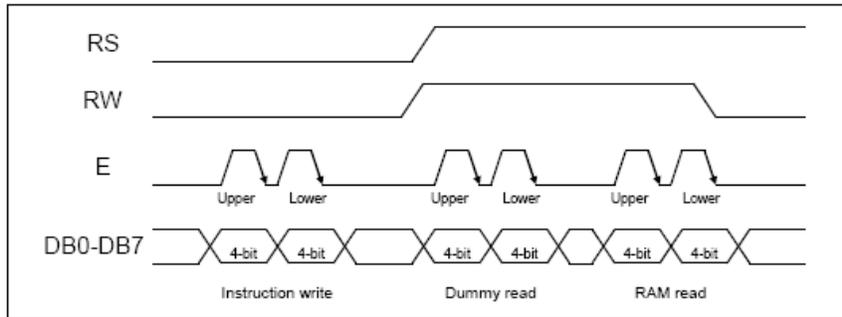
■ **Parallel interface:**

The LCD module is in parallel mode by pulling up PS B pin. The LCD module can select 8-bit or 4-bit bus interface by setting the DL control bit in "Function Set" instruction. MPU can control RS, RW, E and DB0...DB7 pins to complete the data transmission.

In 4-bit transfer mode, every 8-bit data or instruction is separated into 2 parts. The higher 4 bits (bit -7~bit-4) data will be transferred first through data pins (DB7~DB4). The lower 4 bits (bit -3~bit-0) data will be transferred second through data pins (DB7~DB4). The (DB3~DB0) data pins are not used during 4-bit transfer mode.



Timing Diagram of 8-bit Parallel Bus Mode Data Transfer



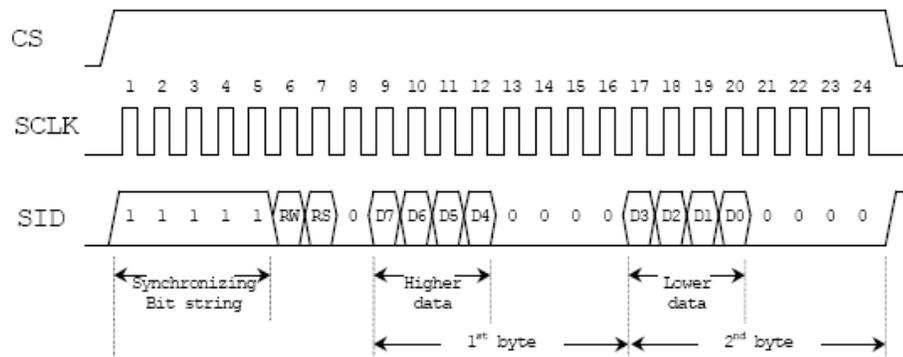
Timing Diagram of 4-bit Parallel Bus Mode Data Transfer

■ **Serial Interface & Transferring Serial Data**

The LCD module enters serial mode when the PSB pin is set low. A two-line clock synchronous transfer method is used. The module receives serial input data (SID) by synchronizing with a transfer clock (SCLK) sent from the master side. When the st7920 interfaces with several chips, chip select pin (CS) must be used. The transfer clock (SCLK) input is activated by making chip select (CS) high. In addition, the transfer counter of the st7920 can be reset and serial transfer synchronized by making chip select (CS) low. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single module interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS) should be fixed to high.

the transfer clock(SCLK) is independent of operational clock of the LCD module. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock must be considered since the st7920 does not have an internal transmit/receive buffer. Following figure shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1(synchronizing bit string) at the beginning of the start byte, the transfer counter of the st7920 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string(5 bits) specify transfer direction(R/W bit) and register select(RS bit). Be sure to transfer 0 in the 8 bit.

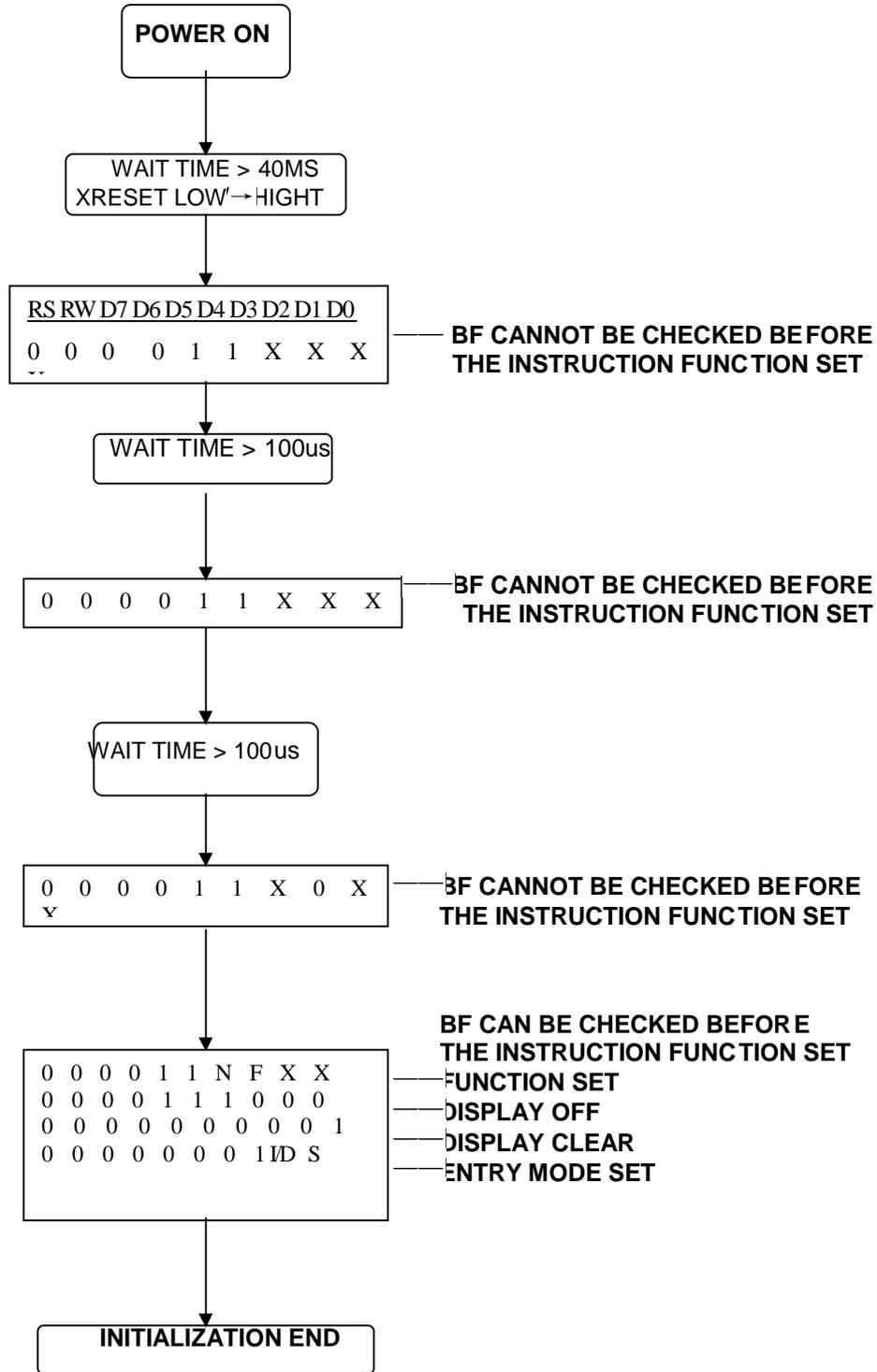
After receiving the start synchronizing bit string, the R/W bit (=0), and RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the higher 4 bits of the instruction are placed in the lsb of the first byte, and the lower 4 bits of the instruction are placed in the lsb of the second byte. Be sure to transfer 0 in the following 4 bits of each byte.



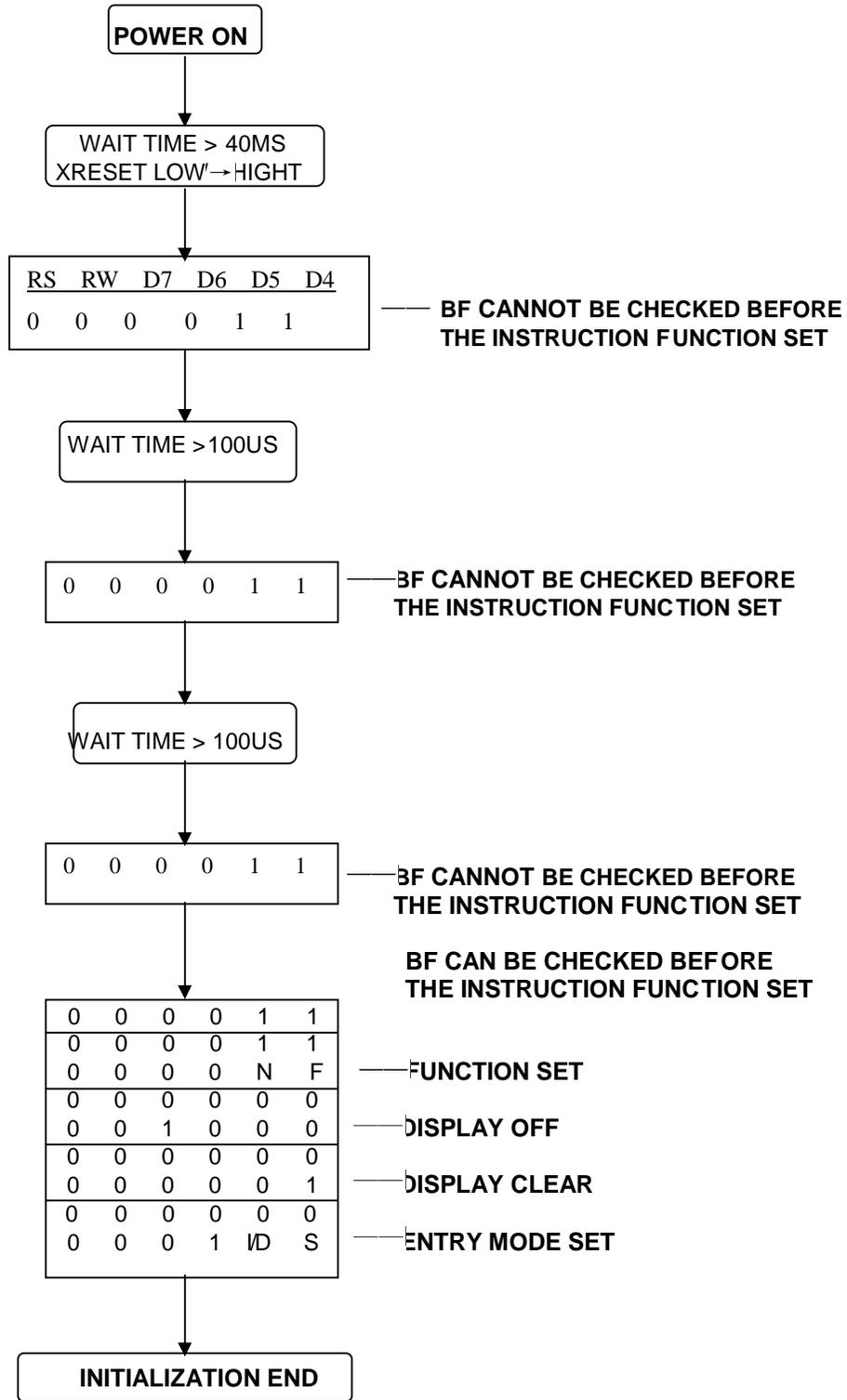
Timing Diagram of Serial Mode Data Transfer

2. INITIALIZING BY INSTRUCTION

- 8-BIT INTERFACE:



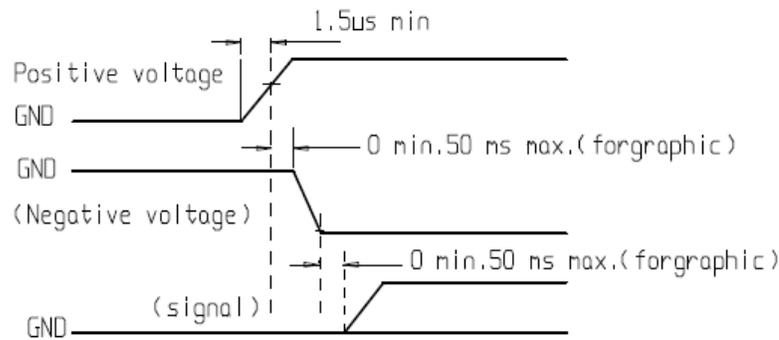
● 4-BIT INTERFACE



Product	Font Type
ST7920-0A	BIG-5 code traditional character set
ST7920-0B	GB code simplified character set
ST7920-0C	GB code,BIG-5 code and Japanese code

LCM Operation Precautions

- (1) It is an indispensable condition to drive LCD within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. An electrochemical reaction due to direct current causes LCD's undesirable deterioration, so that the use of direct current driver should be avoided.
- (2) Response time will be extremely delayed at lower temperature than the specified operating temperature range and on the other hand LCD's show dark blue color in the higher temperature. However, those phenomena do not mean any malfunction or display out of order with LCD's, which will come back in the specified operation temperature range.
- (3) If the display area is pushed hard during operation, some fonts will be abnormally displayed. But it resumes normal condition after turning off once.
- (4) A slight dew depositing on terminals could be a cause for electrochemical reaction resulting in terminal open circuit.
- (5) Display contrast varies with the change of liquid crystal driving voltage (V_o). Adjust V_o to show the best contrast.
- (6) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit. Therefore, it is suggested to use the LCD under the relative condition of 40°C, 85% RH.
- (7) When turning the power on, input each signal after the positive/negative voltage becomes stable.



- (8) The backlight must be operated within the condition of specification. The overload current or too high voltage will reduce the life time or destroy the backlight.

Handling Precautions

- (1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.
- (2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.
- (3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.
- (4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Please handle the polarizer carefully.
- (5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :
 - Isopropyl alcohol
 - Ethyl alcohol
- (6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water

Ver: A

- Ketone

- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the IO cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.

- Tools required for assembling, such as soldering irons, must be properly grounded.

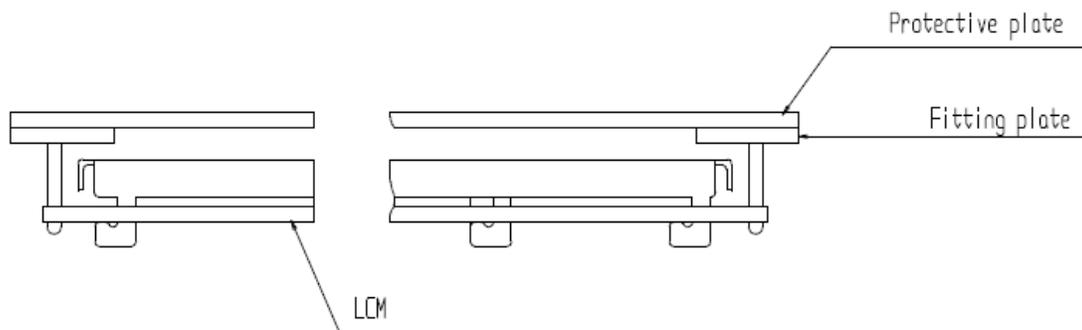
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.

- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

Installing Precautions

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be 0.1mm.

Storage Precautions

In case of storing for a long period of time for the purpose of replacement use, the following ways are recommended.

(1) Storage in a polyethylene bag with the opening sealed so as not to enter fresh air outside in it, and with no desiccant.

(2) Placing in a dark place where neither exposure to direct sunlight nor light is, keeping temperature in the range from -30°C to 80°C

(3) Storing with no touch on polarizer surface by anything else . (It is recommended to store them as they have been contained in the inner container at the time of delivery from us.)

Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leaks out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or

the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature. If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability. To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity

etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.