A M O T E C

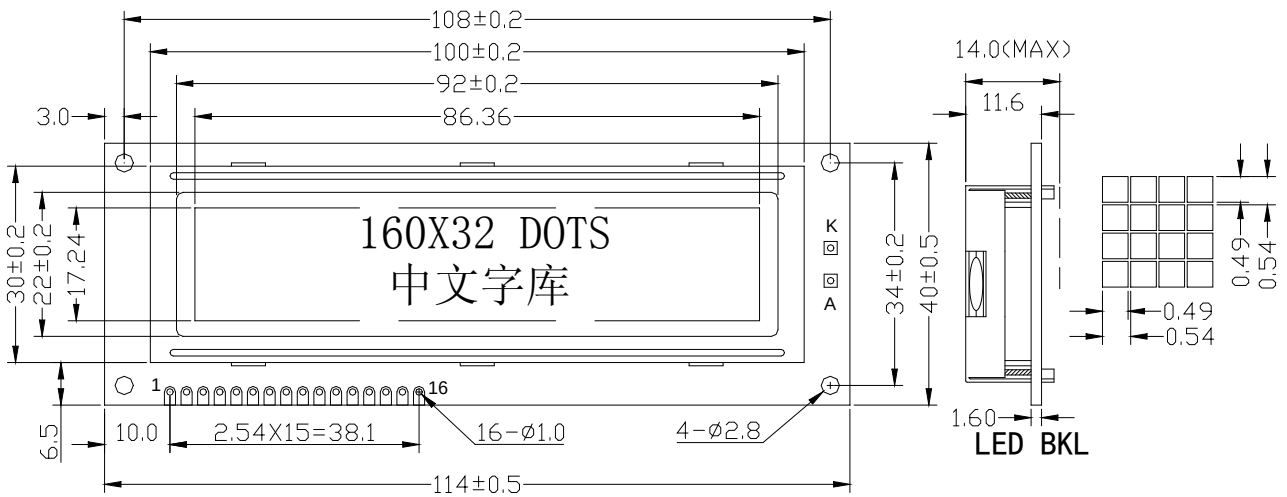
# *ADM16032A*

**SPECIFICATIONS OF LCD MODULE**

## Features

1、 160x32 dots with 8192 chinese character fonts (16x16)
2、 128 alpha-numerical fonts (16x8)
3、 64x256 bit graphic display RAM
4、 Strong display control functions:
Vertical scroll, horizontal bit scroll, line reverse etc
5、 +2.7v~+5.5v power supply
6、 1/32 duty, LED BKL
7、 4 bit, 8 bit, serial interface

## Outline dimension

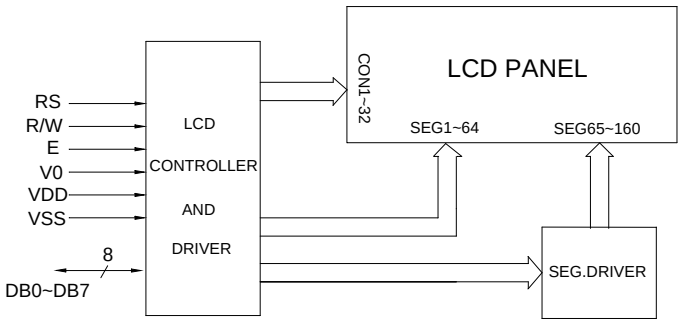


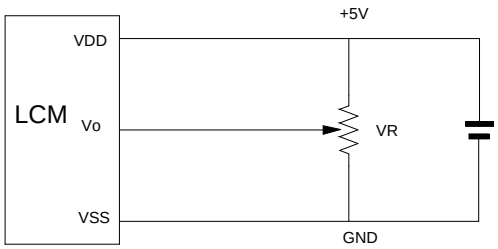

## Absolute maximum ratings

| Item | Symbol | Standard | | | Unit |
|---|---|---|---|---|---|
| Power voltage | $V_{DD}$-$V_{SS}$ | 0 | - | 7.0 | V |
| Input voltage | VIN | VSS | - | VDD | |
| Operating temperature range | VOP | 0 | - | +50 | ℃ |
| Storage temperature range | VST | -20 | - | +60 | |

*****Wide temperature range is available
(operating/storage temperature as –20~+70/-30~+80℃)

## Block diagram




VDD-Vo:LCD DRIVING VOLTAGE
VR:10K~20K

## Interface pin description

| Pin no. | Symbol | External connection | Function |
|---|---|---|---|
| 1 | $V_{SS}$ | Power supply | Signal ground for LCM (GND) |
| 2 | $V_{DD}$ | | Power supply for logic (+5V) for LCM |
| 3 | $V_0$ | | Contrast adjust |
| 4 | RS | MPU | Register select signal |
| 5 | R/W | MPU | Read/write select signal |
| 6 | E | MPU | Operation (data read/write) enable signal |
| 7~10 | DB0~DB3 | MPU | Four low order bi-directional three-state data bus lines.<br>Used for data transfer between the MPU and the LCM.<br>These four are not used during 4-bit operation. |
| 11~14 | DB4~DB7 | MPU | Four high order bi-directional three-state data bus lines.<br>Used for data transfer between the MPU |
| 15 | LED+ | LED BKL power supply | Power supply for BKL (+4.2V) |
| 16 | LED- | | Power supply for BKL (GND) |

## Optical characteristics

STN type display module (Ta=25℃, VDD=5.0V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Viewing angle | θ | $C_r \geqslant 2$ | -60 | - | 35 | deg |
| | Φ | | -40 | - | 40 | |
| Contrast ratio | $C_r$ | | - | 6 | - | - |
| Response time (rise) | $T_r$ | - | - | 150 | 250 | ms |

| | | | | | | |
|---|---|---|---|---|---|---|
| Response time (fall) | $T_r$ | - | - | 150 | 250 | |

## Electrical characteristics

DC characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply voltage for LCD | $V_0$-$V_{ss}$ | Ta =25℃ V=+5V | - | 6.5 | - | V |
| Input voltage | $V_{DD}$ | V=+3.3V | 2.7 | 3.3 | 5.5 | |
| | | V=+5V | 4.7 | 5.0 | 5.5 | |
| Supply current | $I_{DD}$ | Ta=25℃, $V_{DD}$=5.0V | - | 2 | 4 | mA |
| Input leakage current | $I_{LKG}$ | | - | - | 1.0 | uA |
| "H" level input voltage | $V_{IH}$ | | 2.2 | - | $V_{DD}$ | V |
| "L" level input voltage | $V_{IL}$ | Twice initial value or less | 0 | - | 0.6 | |
| "H" level output voltage | $V_{OH}$ | LOH=-0.25mA | 2.4 | - | - | |
| "L" level output voltage | $V_{OL}$ | LOH=1.6mA | - | - | 0.4 | |
| Backlight supply voltage | $V_F$ | | - | 4.2 | 4.6 | |

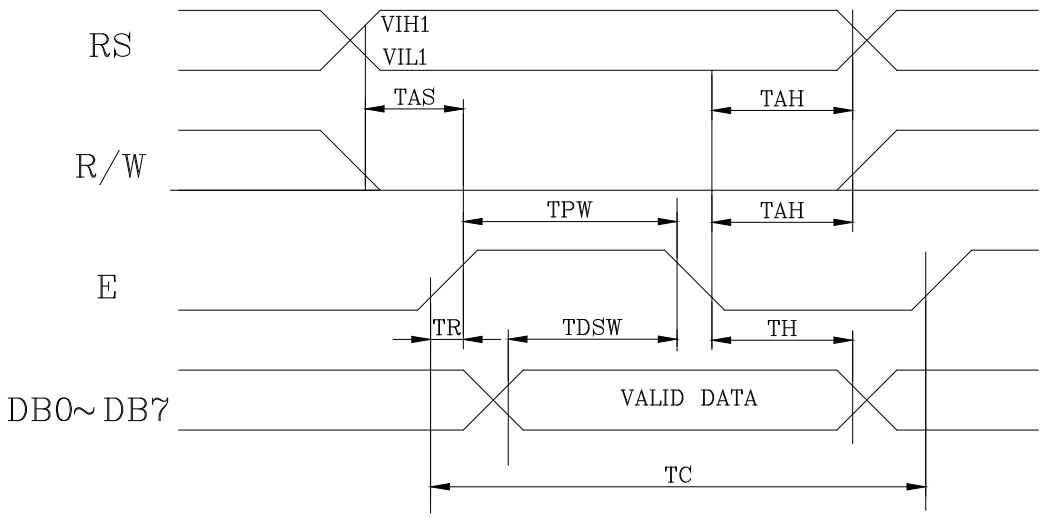
AC Characteristics(VDD=5V,Ta=25℃)

| Symbol | characteristics | Test condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Fosc | OSC frequency | Rf=39k | 480 | 540 | 600 | KHZ |

Write mode (writing data from mpu to st7920)

| parameter | symbol | mesure time | unit |
|---|---|---|---|
| system cycle time | TC | 13,000 | ns |
| address setup time | tas | 1,500 | ns |
| Address hold time | TAH | 1,500 | ns |
| Data setup time | TDSW | 1,000 | ns |
| Data hold time | TH | 20 | ns |
| Enable pulsewidth | TPW | 1,500 | ns |
| Enable rise/fall time | TR,TF | 25 | ns |

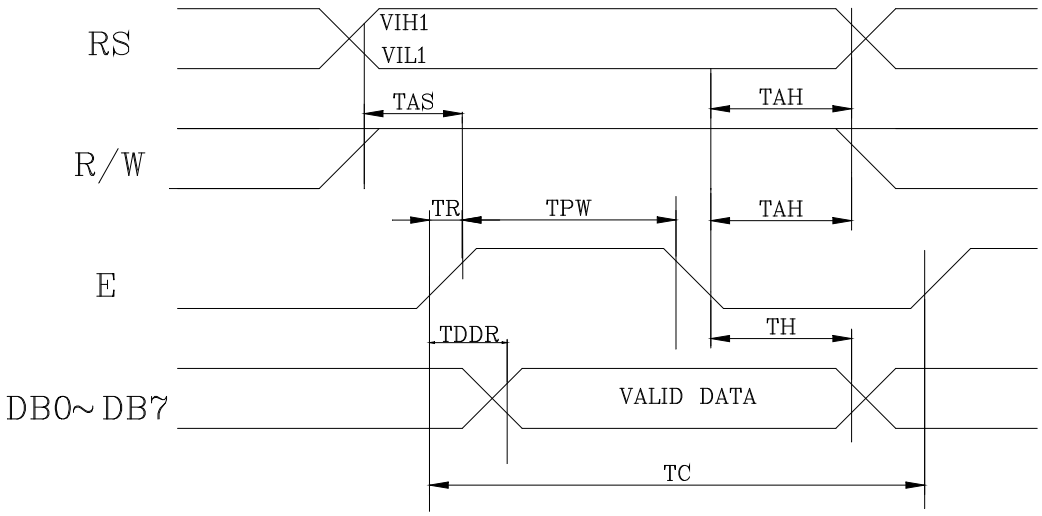
Write Timing



Read mode(READING DATA FORM ST7920 TO MPU)

| parameter | symbol | mesure time | unit |
|---|---|---|---|
| system cycle time | TC | 13,000 | ns |
| address setup time | tas | 1,500 | ns |
| Address hold time | TAH | 1,500 | ns |
| Data setup time | TDDR | 1,000 | ns |
| Data hold time | TH | 20 | ns |
| Enable pulsewidth | TPW | 1,500 | ns |
| Enable rise/fall time | TR,TF | 25 | ns |

Read timing




## Character Generator ROM (CGROM)

The character generator ROM generates 16 x 16 dot or 16 x 8 dot character patterns from two 8 -bit character codes. User-defined character patterns are also available by mask -programmed ROM.

## Character Generator RAM (CGRAM)

In the character generator RAM, the user can rewrite character patterns by program. For 16 x 16 dots, four character patterns can be written.

See Table 1 for the relationship between CGRAM addresses and data and display patterns. Areas they are not used for display can be used as general data RAM.

## Timing Generation Circuit

The timing generation circuit generates timing signals for the operation of internal circuits such as DDRAM, CGROM and CGRAM. RAM read timing for display and internal operation timing by MPUaccess are generated separately to avoid interfering with each other. Therefore, when writing data toDDRAM, for example, there will be no undesirable interference, such as flickering, in areas other

thanthe display area.

## LCD Driver Circuit

LCD Driver circuit has 33 common and 64 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to 64 bit segment latch serially, and then it is stored to 64 bit shift latch. When each common is selected by 33 bit common register, segment data also output through segment driver from 64 bit segment latch.

## Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor/blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

| Character code DDRAM data | | | | | CGRAM Address | | | | | | CGRAM Data High byte | | | | | | | | CGRAM Data Low byte | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B15~B4 | B3 | B2 | B1 | B0 | B5 | B4 | B3 | B2 | B1 | B0 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0 | X | 0 | 0 | X | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | X | 0 | 1 | X | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | 0 | 0 | 0 |
| | | | | | | | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 0 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 1 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 0 | 1 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 0 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | **1** | **1** | **1** | **1** | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 1 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| | | | | | | | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Table1** Relationship Between Cgram Addresses, Character Codes(Ddram) And Character Patterns (Cgram Data)

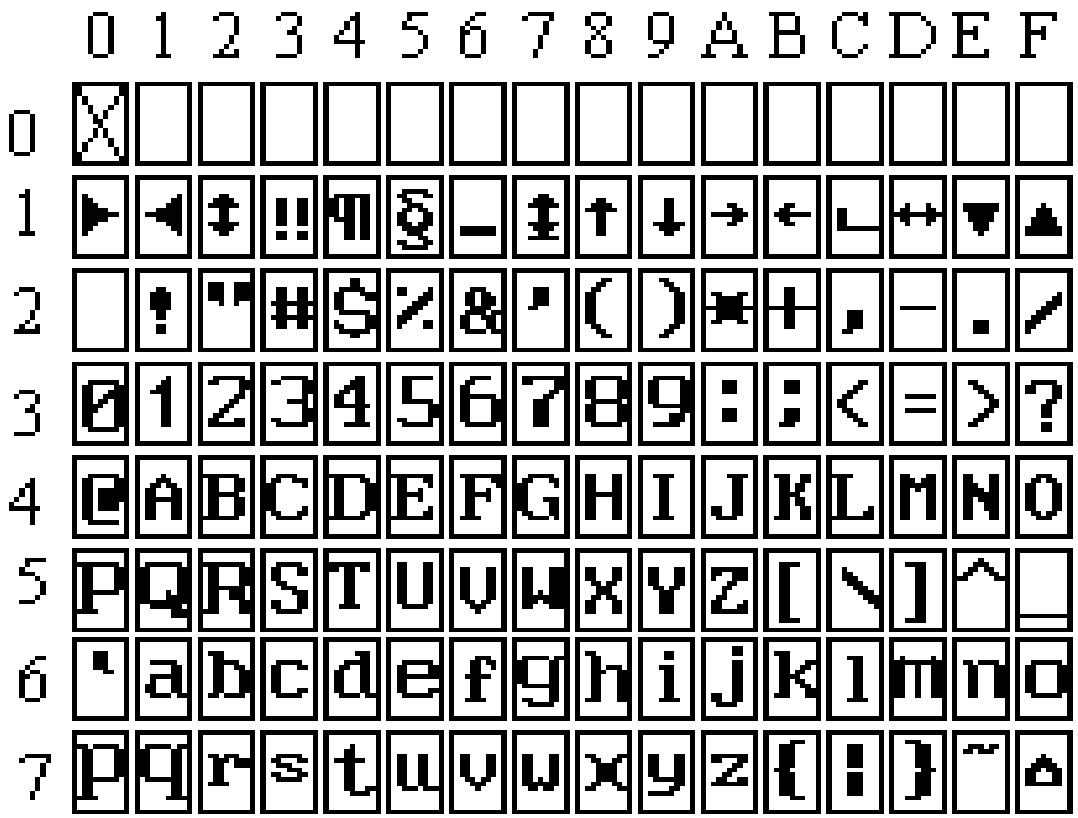
## Notes:

1. Character Code Bits 1 To 2 Correspond To Cgra m Address Bits 4 To 5 (2 Bit: 4 Types).
2. Cgram Address Bits 0 To 3 Designate The Character Pattern Line Position. The 16th Line Is The Cursor Position And A Logical Or With The Cursor Forms Its Display. Maintain The 16th Line Data,Correspo-Nding To The Cursor Display Position, As To As The Cursor Display. If The 16th Line Data Is 1,1 Bits Will Light Up The 16th Line Regardless Of The Cursor Presence.
3. Character Pattern Row Positions Correspond To Cgram Data Bits 0 To 15(Bit 15 Being At The Left).

***4.As Shown Table, Cgram Character Patterns Are Selected When Character Code Bits 4 To 15 Are All 0 and Bit 0 And bit 3 are Don└┘T Care(X).**

**Table 2** Relationship Between Icon Ram Addresses,Data And Segment Pin Location Bit Map.

| | | ICON RAM Data | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | high Byte | | | | | | | | low byte | | | | | | | |
| icon ram address(ac3——ac0) | | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| | 0 | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | SEG8 | SEG9 | SEG10 | SEG11 | SEG12 | SEG13 | SEG14 | SEG15 |
| | 1 | SEG16 | SEG17 | SEG18 | SEG19 | SEG20 | SEG21 | SEG2 | SEG23 | SEG24 | SEG25 | SEG26 | SEG27 | SEG28 | SEG29 | SEG30 | SEG31 |
| | 2 | SEG32 | SEG33 | SEG34 | SEG35 | SEG36 | SEG37 | SEG38 | SEG39 | SEG40 | SEG41 | SEG42 | SEG43 | SEG44 | SEG45 | SEG46 | SEG47 |
| | 3 | SEG48 | SEG49 | SEG50 | SEG51 | SEG52 | SEG53 | SEG54 | SEG55 | SEG56 | SEG57 | SEG58 | SEG59 | SEG60 | SEG61 | SEG62 | SEG63 |
| | 4 | SEG64 | SEG65 | SEG66 | SEG67 | SEG68 | SEG69 | SEG70 | SEG71 | SEG72 | SEG73 | SEG74 | SEG75 | SEG76 | SEG77 | SEG78 | SEG79 |
| | 5 | SEG80 | SEG81 | SEG82 | SEG83 | SEG84 | SEG85 | SEG86 | SEG87 | SEG88 | SEG89 | SEG90 | SEG91 | SEG92 | SEG93 | SEG94 | SEG95 |
| | 6 | SEG96 | SEG97 | SEG98 | SEG99 | SEG100 | SEG101 | SEG102 | SEG103 | SEG104 | SEG105 | SEG106 | SEG107 | SEG108 | SEG109 | SEG110 | SEG111 |
| | 7 | SEG112 | SEG113 | SEG114 | SEG115 | SEG116 | SEG117 | SEG118 | SEG119 | SEG120 | SEG121 | SEG122 | SEG123 | SEG124 | SEG125 | SEG126 | SEG127 |
| | 8 | SEG128 | SEG129 | SEG130 | SEG131 | SEG132 | SEG133 | SEG134 | SEG135 | SEG136 | SEG137 | SEG138 | SEG139 | SEG140 | SEG141 | SEG142 | SEG143 |
| | 9 | SEG144 | SEG145 | SEG146 | SEG147 | SEG148 | SEG149 | SEG150 | SEG151 | SEG152 | SEG153 | SEG154 | SEG155 | SEG156 | SEG157 | SEG158 | SEG159 |
| | A | SEG160 | SEG161 | SEG162 | SEG163 | SEG164 | SEG165 | SEG166 | SEG167 | SEG168 | SEG169 | SEG170 | SEG171 | SEG172 | SEG173 | SEG174 | SEG175 |
| | B | SEG176 | SEG177 | SEG178 | SEG179 | SEG180 | SEG181 | SEG182 | SEG183 | SEG184 | SEG185 | SEG186 | SEG187 | SEG188 | SEG189 | SEG190 | SEG191 |
| | C | SEG192 | SEG193 | SEG194 | SEG195 | SEG196 | SEG197 | SEG198 | SEG199 | SEG200 | SEG201 | SEG202 | SEG203 | SEG204 | SEG205 | SEG206 | SEG207 |
| | D | SEG208 | SEG209 | SEG210 | SEG211 | SEG212 | SEG213 | SEG214 | SEG215 | SEG216 | SEG217 | SEG218 | SEG219 | SEG220 | SEG221 | SEG222 | SEG223 |
| | E | SEG224 | SEG225 | SEG226 | SEG227 | SEG228 | SEG229 | SEG230 | SEG231 | SEG232 | SEG233 | SEG234 | SEG235 | SEG236 | SEG237 | SEG238 | SEG239 |
| | F | SEG240 | SEG241 | SEG242 | SEG243 | SEG244 | SEG245 | SEG246 | SEG247 | SEG248 | SEG249 | SEG250 | SEG251 | SEG252 | SEG253 | SEG254 | SEG255 |



## Display command

The ST7920 which have two categories of instructions that:

## Instruction Tabe: (RE=0:Enable basic instruction.)

| Parameter | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Note | Execution time (450khz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Clear Display | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Write “20h”To Ddram And Set Ddram Address To”00h” From Ac | 2.5ms |
| Return home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | X | Set Ddram Address To "00h" From Ac And Return Cursor To Its Original Position If Shifted.The Contents Of Ddram Are Not Change | 2.5ms |
| Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets Cursor Move Direction And Specifies Display Shift. These Operations Are Performed During Data Write And Read | 60μs |
| Display on/off | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | D=1:Entire Display On<br>C=1:Cursor On<br>B=1:Cursor Position On | 60μs |
| Cursor or Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | X | X | Set Cursor Moving And Display Shift Control Bit, And The Direction Without Changing Ddram Data | 60μs |
| Function Set | 0 | 0 | 0 | 0 | 1 | DL | N | 0<br>RE | G | X | Dl:Interface Data Is 8/4 Bits<br>N=1 & Re=0: 3 Line Setting<br>N=1 & Re=1: 4 Line Setting<br>G=1: Graphic Display On<br>G=0: Graphic Display Off<br>Others: 2 Line Setting<br>Re=1: Extended Instruction Setting<br>Re=0: Normal Instruction Setting | 60μs |
| Set CGRAM Address | 0 | 0 | 0 | 1 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set Cgram Address In Address Cornter | 60μs |
| Set DDRAM Address | 0 | 0 | 1 | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Set Ddram Address In Address Cornter | 60μs |
| Read Busy Flug and Address | 0 | 1 | BF | AC6 | AC5 | AC4 | AC3 | AC2 | AC1 | AC0 | Wether During Internal Operation Or Not Can Be Known By Reading Bf . The Cintents Of Address Counter Can Also Be Read. | 0μs |
| Write Data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Write Data Into Internal Ram | 60μs |
| Read Data | 1 | 1 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Read Data From Internal Ram | 60μs |

## Instruction Table: (RE=1: Enable extension instruction.)

| Parameter | RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Note | Execution time (450khz) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Standby Mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Enter Standby Mode, Only Icon Areas Display. Standby Mode Can Be Released By Any Other Instructions. | 60 us |
| Start Row Enable | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | SR | Sr=1: Allow Change Start Display Row. Sr=0: Disable Start Display Row Change. | 60us |
| Reverse Line Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | R1 | R0 | Choice One Of 4 Lines Which Data Is Reverse Display. | 60 μ s |
| Sleep mode and Set GRAM page | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Sl=0: Enter Sleep Mode.<br>Sl=1: Wake-Up From Sleep Mode<br>Gd: Display Graphic Page 0 Or 1<br>Gw: Write Data To Graphic Page 0 Or 1. (Effective While Gp=1) | 60 μ s |
| Display Shift by dot | 0 | 0 | 0 | 0 | 0 | 1 | OA | LR | L1 | L0 | Oa=1: One Of 4 Lines Shift Enable.<br>Oa=0: All Line Shift Enable.<br>Lr=1: Dot By Dot Shift Right.<br>Lr=0: Dot By Dot Shift Left.<br><br>L1,L0: Choice One Of 4 Lines Shift | 60 μ s |
| Function Set (Modify) | 0 | 0 | 0 | 0 | 1 | CL | N | 1<br>RE | G | GP | Cl=1: Select 16 Character Line<br>Cl=0: Select 8 Character Line<br>N=1 & Re=1: 4 Line Display<br>Re=1: Extended Instruction Setting. Re=0: Normal Instruction Setting.<br>G=1: Graphic Display On<br>G=0: Graphic Display Off<br>Gp=1: Two Page Gram<br>Gp=0: One Page Gram | 60 μ s |
| Set IRAM or Start Row address | 0 | 0 | 0 | 1 | AC 5 | AC 4 | AC 3 | AC 2 | AC 1 | AC 0 | Sr=1: Ac5~Ac0 Is Start Row<br>Sr=0: Ac5~Ac0 Is Icon Ram Address | 60 μ s |
| Set Graphic RAM address | 0 | 0 | 1 | AC 6 | AC 5 | AC 4 | AC 3 | AC 2 | AC 1 | AC 0 | Set Graphic Ram Address In Address Counter. Execute Once Set The Address Of Display Row. Execute Again Set The Address Of Display Column. Each Address Of Display Column Has Data Of 16 Bits. Therefore Write Data Should Execute 2 Times. | 60 μ s |

**NOTE:**

Be sure the st7920 is not in the busy state (bf = 0) before sending an instruction from the mpu to

The st7920. if an instruction is sent without checking the busy flag, the time between the

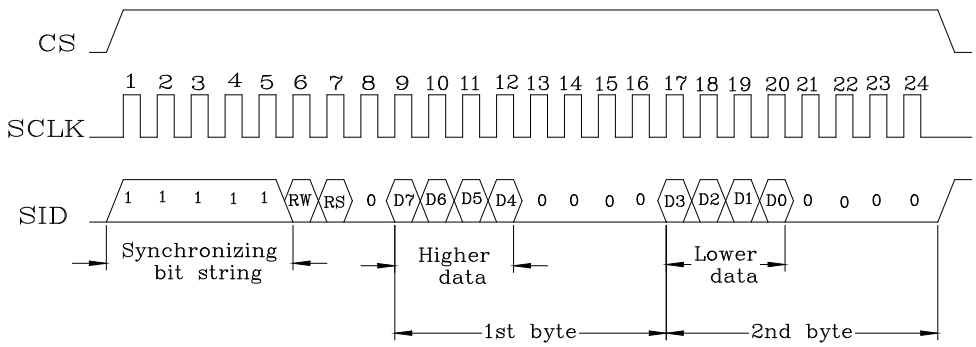
first instruction and next instruction will take much longer than the instruction time itself. Refer to instruction table for the list of each instruction execution time.

## 1. Serial Interface & Transferring Serial Data

The st7920 enters serial mode when the psb pin is set low. A two -line clock synchronous transfer method is used. The st7920 receives serial input data(sid) by synchronizing with a transfer clock(sclk) sent fro m the master side. When the st7920 interfaces with several chips, chip select pin(cs) must be used. The transfer clock(sclk) input is activated by making chip select(cs) high. In addition, the transfer counter of the st7920 can be reset and serial transfer synchronized by making chip select(cs) low. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single st7920 interfaces to a single mpu, an interface can be con structed from the transfer clock(sclk) and serial input data(sid). In this case, chip select(cs) should be fixedto high.

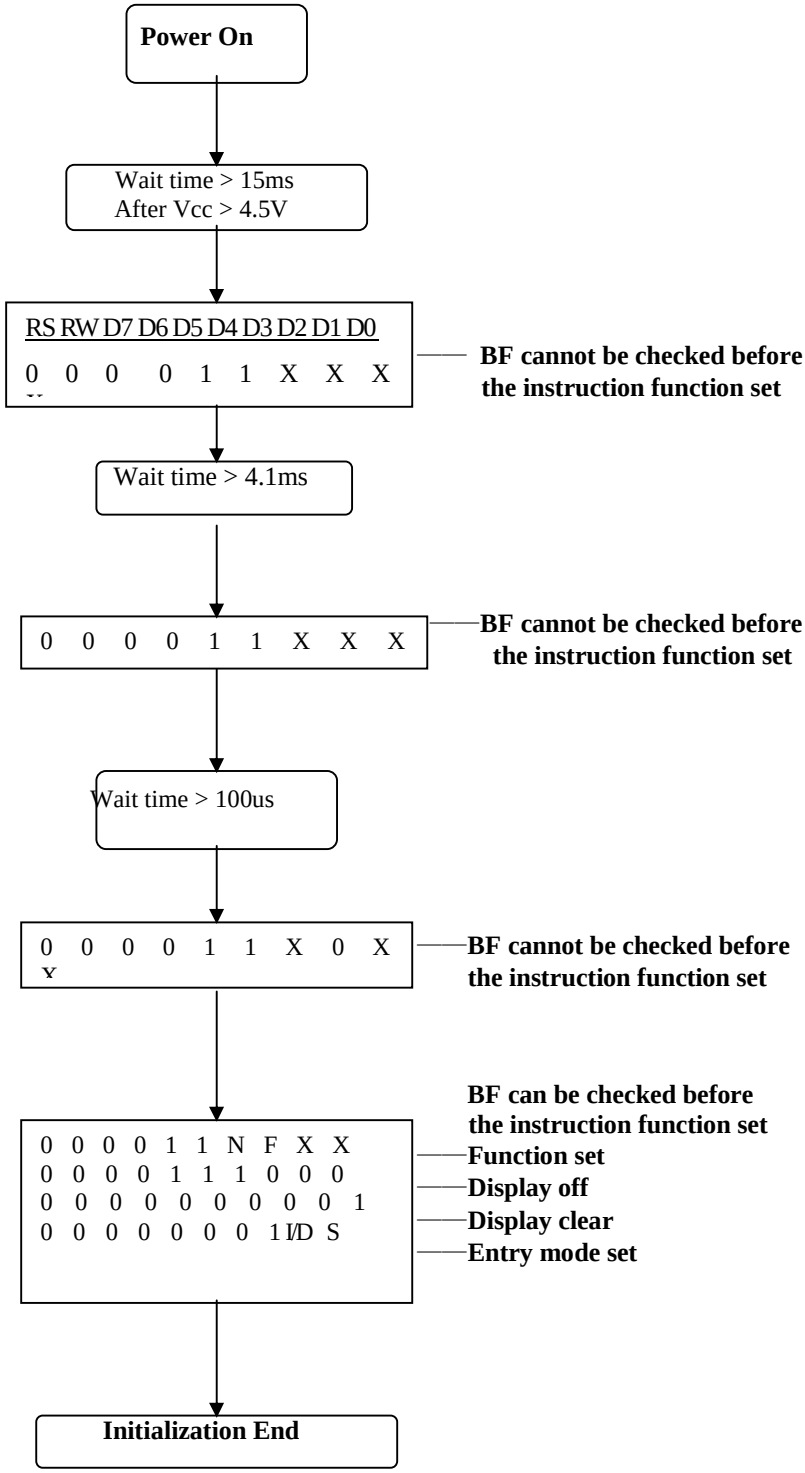
the transfer clock(sclk) is independent of operational clock of the st7920. however, when several instructions are continuously tra nsferred, the instruction execution time determined by the operational clock must be considered since the st7920 does not have an internal transmit/receive buffer. Following figure shows the basic procedure for transferring serial data. To begin with, tran sfer the start byte. By receiving five consecutive bits of 1(synchronizing bit string) at the beginning of the start byte, the transfer counter of the st7920 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string(5 bits) specify transfer direction(rw bit) and register select(rs bit). Be sure to transfer 0 in the 8 th bit.

After receiving the start synchronizing bit string, the rw bit(=0), and rs bit in the start byte, an 8-bit instruction is received in 2 bytes: the higher 4 bits of the instruction are placed in the lsb of the first byte, and the lower 4 bits of the instruction are placed in the lsb of the second byte. Be sure to transfer 0 in the following 4 bits of each byte.

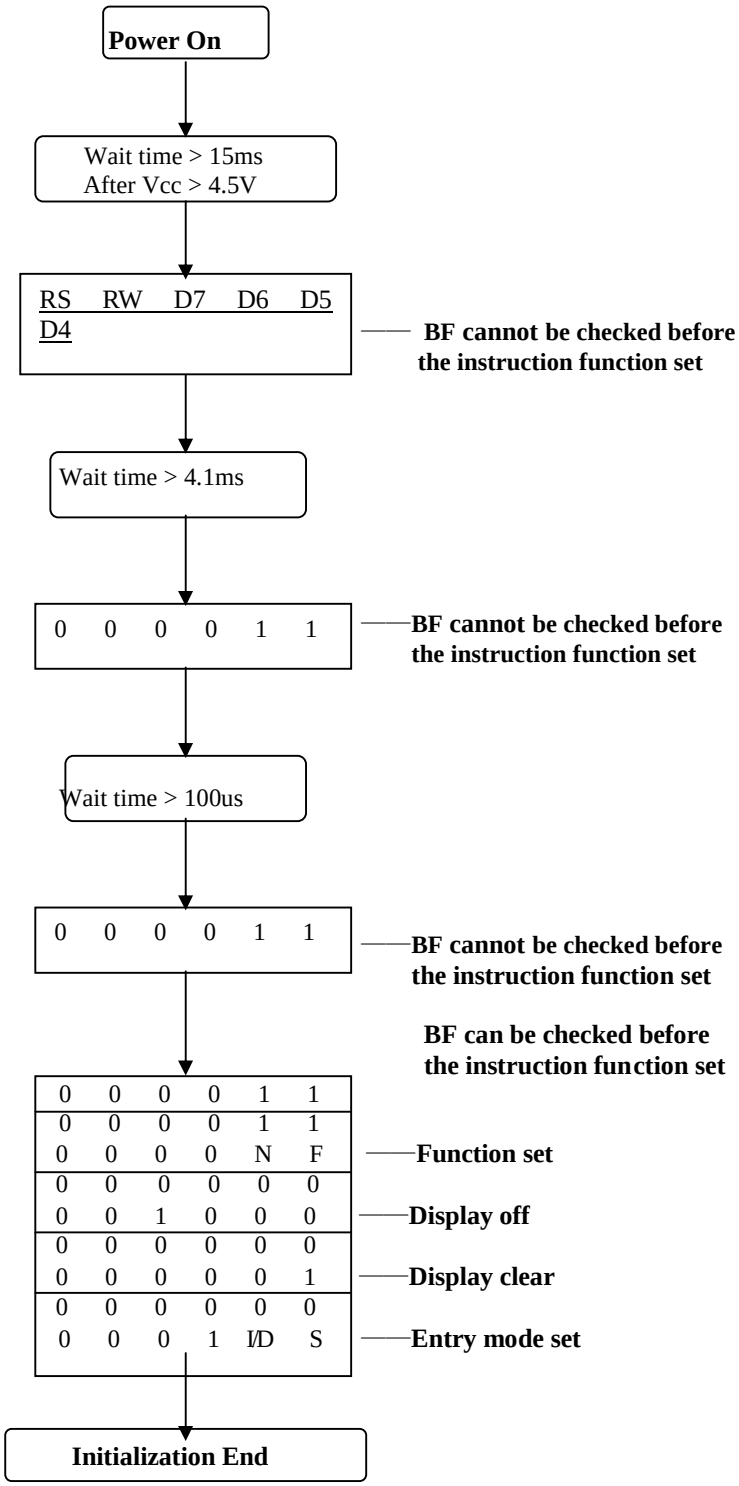


## 2. Initializing by instruction

- 8-bit Interface:



- **4-bit Interface**



# ST7920 BIG-5 中文字型码表