Thin-Film-Transistor LCD Module
Model:XTPQ28NN08-02

Acceptance

Approved and Checked by

Approved by	Checked by		Made by

Revise Records

Rev.	Date	Contents	Written	Approved
A	2017/04/24	Preliminary Specification	GAO	JACK

Special Notes

Note1.	
Note2.	
Note3.	
Note4.	
Note5.	

1.General Description and Features

XTPQ28NN08-02 is a TM (Transmissive) type color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT-LCD module, a driver circuit and a back-light unit . The resolution of a 2.8" contains 240RGBx320 dots and can display up to 262K colors. The following table described the features of XTPQ28NN08-02.

LCD Module

Item	Specification	Unit
Screen Size	2.8inches	Diagonal
Display Resolution	240RGB(H)x320(V)	Dot
Active Area	43.2(H) x57.6 (V)	mm
Outline Dimension	50.2(W) x 69.3 (H) x 4.0 (D)	mm
Display Mode	Normally white/Transmissive	--
Pixel Arrangement	RGB-Vertical Stripe	--
Display Color	262K	--
Gray scale inversion Direction	12 o'clock	
Viewing Direction	6 o'clock	--
Brightness	300cd/m2	
Drive IC	ILI9341V	--

2.Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	--	50.2	--	mm	--
	Vertical (V)	--	69.3	--	mm	(1)
	Thickness (T)	--	4.0	--	mm	(2)
Weight		--	N/A	--	g	--

Note (1) Not include FPC.
Refer to the Outline Dimension for further information.
(2) Back-light unit are included.

3.Electrical Specifications

3.1 Absolute Max. Ratings

3.1.1 Absolute Ratings of Environment

If the operating condition exceeds the following absolute maximum ratings, the TFT LCD module may be damaged permanently.

(Ta=25±2°C, V_{SS}=GND=0)

Item	Symbol	Min.	Max.	Unit	Note
Operating temperature	T_{OPR}	-20	70	°C	(1)
Storage temperature	T_{STG}	-30	80	°C	(1,2,3)

Note (1) 95 % RH Max. (40 °C ≥ Ta). Maximum wet-bulb temperature at 39 °C or less. (Ta > 40 °C)
No condensation.

Note (2) In case of below 0°, the response time of liquid crystal (LC) becomes slower and the color of panel becomes darker than normal one. Level of retardation depends on temperature, because of LC's character

Note (3) Only operation is guarantied at operating temperature. Contrast, response time, another display quality are evaluated at +25°C.

3.2 Electrical Absolute Rating

3.2.1 TFT-LCD Module

(Voltage Referenced to VSS)

Item	Symbol	Value		Unit	Condition
		Min.	Max.		
Digital Power Supply Voltage	VDD	VSS-0.3	5.0	V	--

3.2.2 Back-Light Unit

(Ta=25±2°C)

Item	Symbol	Min.	Max.	Unit	Note
Current(1LED)	I_f	--	30	mA	(1)
voltage	V_R	--	5	V	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded or reverse voltage is loaded. Functional operation should be restricted to the conditions described under normal operating conditions.

4 Electrical Characteristics

4.1 Backlight Unit

The back-light system is an edge-lighting type with four white LEDs (Light Emitting Diode).

(Ta=25±2°C)

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
LED Voltage	VF	3.0	3.2	3.4	V	
LED Current	IF	-	60	--	mA	
Power Consumption	P_{BL}	-	(192)	-	mW	

Note (1) Where I_F = 60mA, V_F = 3.2, $P_{BL} = V_F \times I_F$

5 Input Terminal Pin Assignment

<table>
<tr><th>PIN.NO</th><th>SYMBOL</th><th>I/O/P</th><th>FUNCTI</th><th>MEMARK</th></tr>
<tr><td>1</td><td>LED K</td><td>P</td><td>POWER FOR BACKLIGHT (GROUN)</td><td></td></tr>
<tr><td>2</td><td>LED A1</td><td>P</td><td>POWER FOR BACKLIGHT(ANODE)</td><td></td></tr>
<tr><td>3</td><td>LED A2</td><td>P</td><td>POWER FOR BACKLIGHT(ANODE)</td><td></td></tr>
<tr><td>4</td><td>LED A3</td><td>P</td><td>POWER FOR BACKLIGHT(ANODE)</td><td></td></tr>
<tr><td>5</td><td>LED A4</td><td>P</td><td>POWER FOR BACKLIGHT(ANODE)</td><td></td></tr>
<tr><td>6</td><td>IM0</td><td rowspan="5">I</td><td rowspan="5">- Select the MCU interface mode
<table>
<tr><th rowspan="2">IM3</th><th rowspan="2">IM2</th><th rowspan="2">IM1</th><th rowspan="2">IM0</th><th rowspan="2">MCU-Interface Mode</th><th colspan="2">DB Pin in use</th></tr>
<tr><th>Register/Content</th><th>GRAM</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[7:0]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[15:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[8:0]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface Ⅰ</td><td>D[7:0]</td><td>D[17:0]</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅰ</td><td colspan="2">SDA: In/OUT</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:10]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface Ⅱ</td><td>D[8:1]</td><td>D[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface Ⅱ</td><td>D[17:10]</td><td>D[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface Ⅱ</td><td colspan="2">SDI: In
SDO: Out</td></tr>
</table>
MPU Parallel interface bus and serial interface select
If use RGB Interface must select serial interface.
* : Fix this pin at VDDI or VSS.</td><td></td></tr>
<tr><td>7</td><td>IM1</td><td></td></tr>
<tr><td>8</td><td>IM2</td><td></td></tr>
<tr><td>9</td><td>IM3</td><td></td></tr>
<tr><td>10</td><td>RST</td><td>I</td><td>This signal will reset the device and must be applied to properly initialize the chip.
Signal is active low.</td><td></td></tr>
<tr><td>11</td><td>VSYN</td><td>I</td><td>Frame synchronizing signal for RGB interface operation.
Fix to VDDI or VSS level when not in use.</td><td></td></tr>
<tr><td>12</td><td>HSYN</td><td>I</td><td>Line synchronizing signal for RGB interface operation.
Fix to VDDI or VSS level when not in use.</td><td></td></tr>
</table>

13	**DCLK**	**I**	Dot clock signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*	
14	**DE**	**I**	Data enable signal for RGB interface operation. *Fix to VDDI or VSS level when not in use.*	
15-32	**DB17-DB0**	**I/O**	18-bit parallel bi-directional data bus for MCU system and RGB interface mode *Fix to VSS level when not in use*	
33	**SDO**	**O**	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin	
34	**SDI**	**I/O**	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.	
35	**RD**	**I**	8080-Ⅰ/8080-Ⅱ system (RDX): Serves as a read signal and MCU read data at the rising edge. *Fix to VDDI level when not in use.*	
36	**D/C（WR）**	**I**	- 8080-Ⅰ/8080-Ⅱ system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. *Fix to VDDI level when not in use.*	
37	**SCL(D/C)**	**I**	This pin is used to select “Data or Command” in the parallel interface or 4-wire 8-bit serial data interface. When DCX = ’1’, data is selected. When DCX = ’0’, command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.	
38	**CS**	**I**	Chip select input pin (“Low” enable). This pin can be permanently fixed “Low” in MPU interface mode only. * note1.2	
39	**TE**	**O**	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.	
40	**VDDI**	**P**	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)	
41	**VDDI**	**P**	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)	
42	**VCI**	**I**	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)	
43	**GND**	**P**	**GROUN**	
44	**X+**		RIGHT ELECTRODE	

45	**Y+**		BOTTOM ELECTRODE	
46	**X-**		LEFT ELECTRODE	
47	**Y-**		TOP ELECTRODE	
48	**GND**	**P**	**GROUN**	
49	**GND**	**P**	**GROUN**	
50	**GND**	**P**	**GROUN**	

6 Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Transmittance (without Polarizer)		T(%)	—	—	17.3	—	—	
Contrast Ratio		CR	Θ=0 Normal viewing angle — —	400	500	—	—	(1)(2)
Response time	Rising	T_R		—	4	8	msec	(1)(3)
	Falling	T_F		—	12	24		
Color gamut		S(%)			60		%	
Color chromaticity (CIE1931)	White	W_x		0.283	0.303	0.323		(1)(4) CF glass (C-light)
		Wy		0.305	0.325	0.345		
	Red	Rx		0.606	0.626	0.646		
		Ry		0.314	0.334	0.354		
	Green	Gx		0.257	0.277	0.297		
		Gy		0.529	0.549	0.569		
	Blue	Bx		0.122	0.142	0.162		
		By		0.102	0.122	0.142		
Viewing angle	Hor.	Θ_L	CR>10	35	45	—		
		Θ_R		35	45	—		
	Ver.	Θ_U		40	50	—		
		Θ_D		10	20	—		

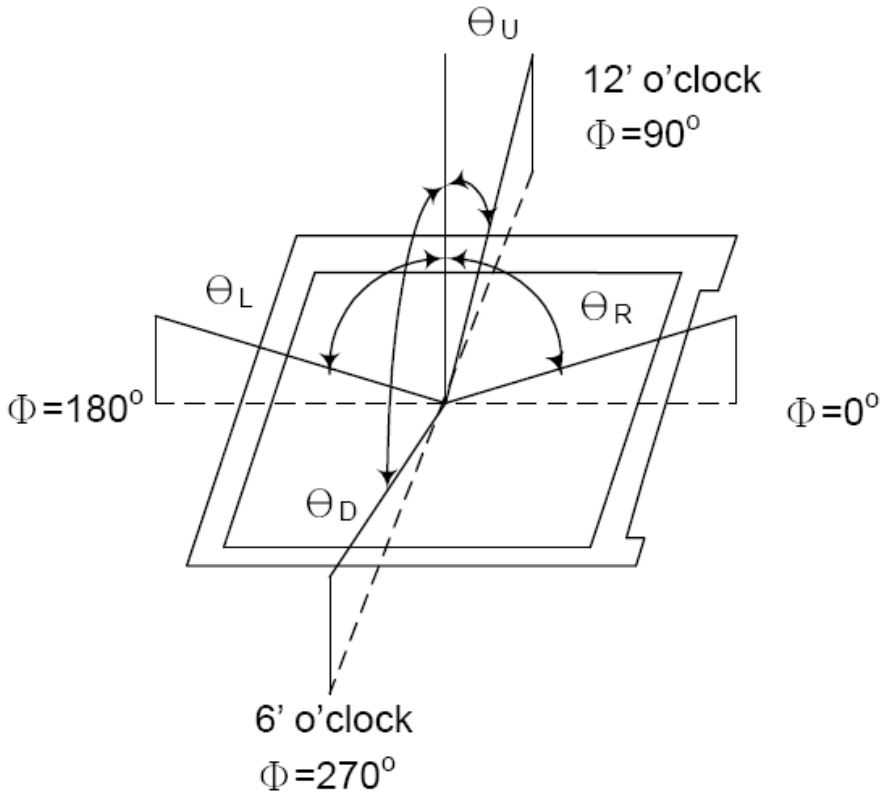
Measuring Condition

- Measuring surrounding : dark room
- Ambient temperature : 25±2°C
- 15min. warm-up time.

Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

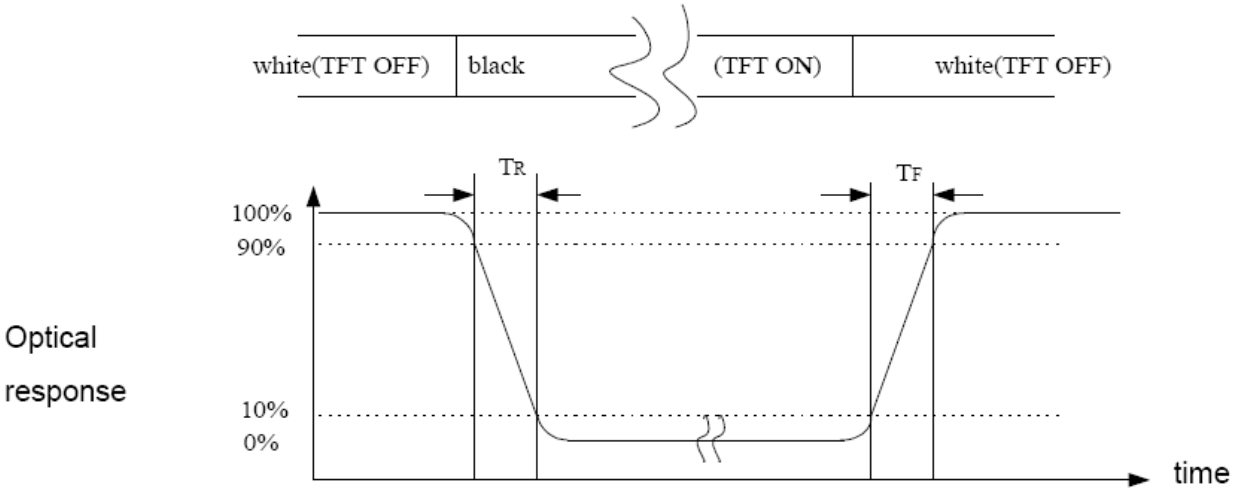
Note (1) Definition of Viewing Angle :



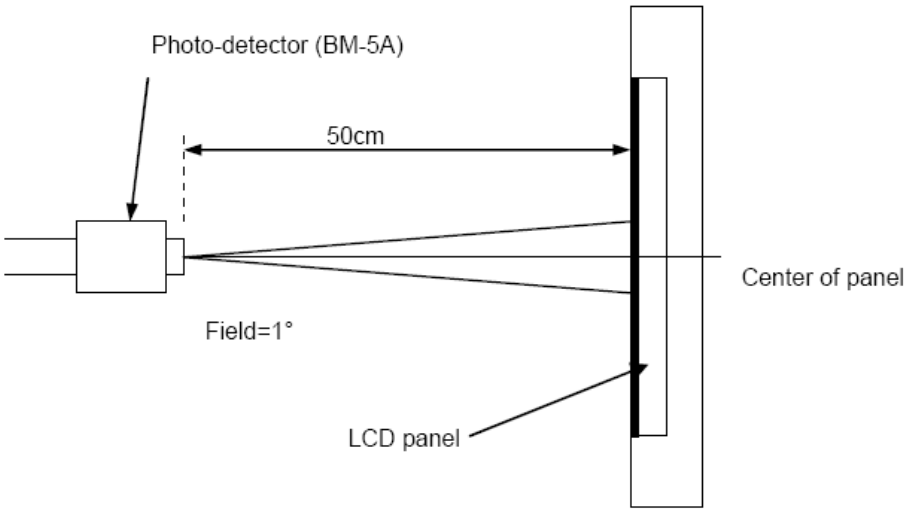
Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F

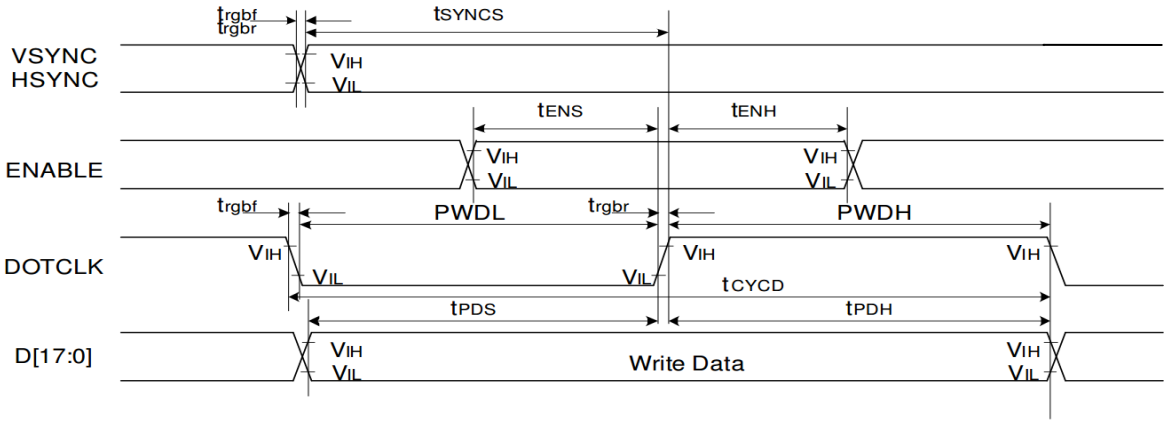


Note (4) Definition of optical measurement setup



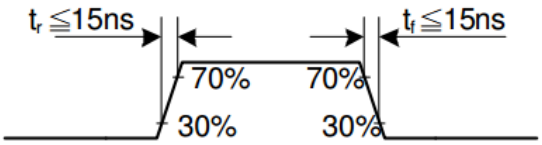
7 Interface Timing

18.3.5 Parallel 18/16/6-bit RGB Interface Timing Characteristics

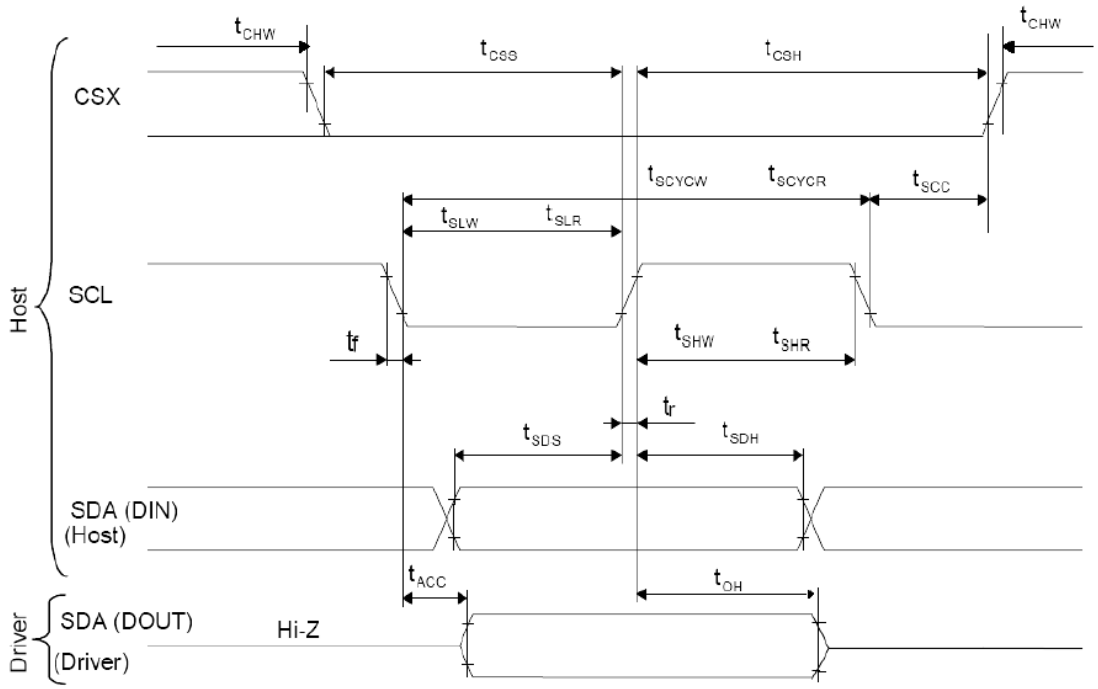


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{POS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

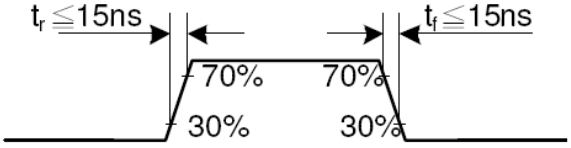


18.3.3 Display Serial Interface Timing Characteristics (3-line SPI system)

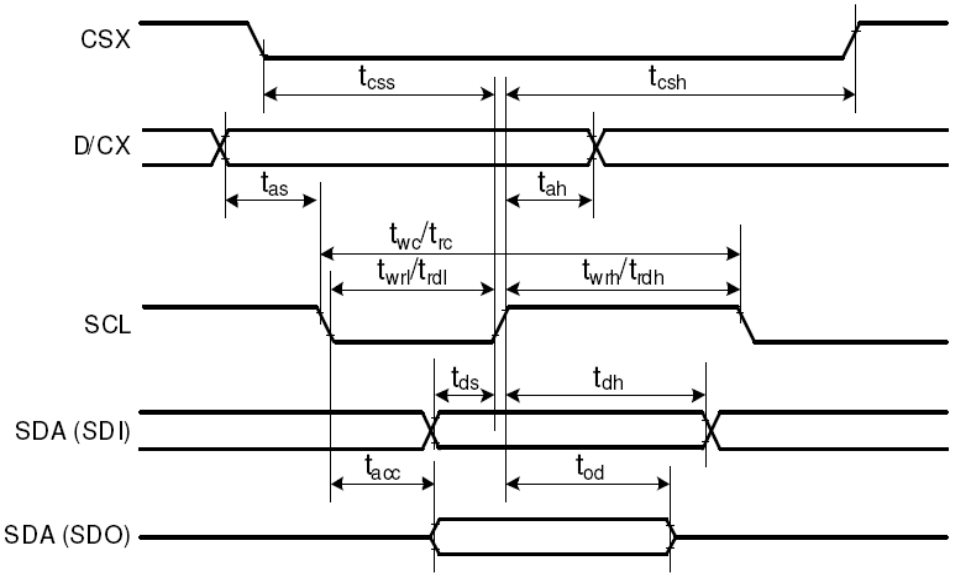


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

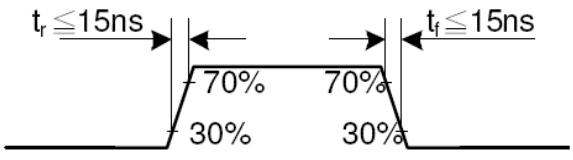


18.3.4 Display Serial Interface Timing Characteristics (4-line SPI system)

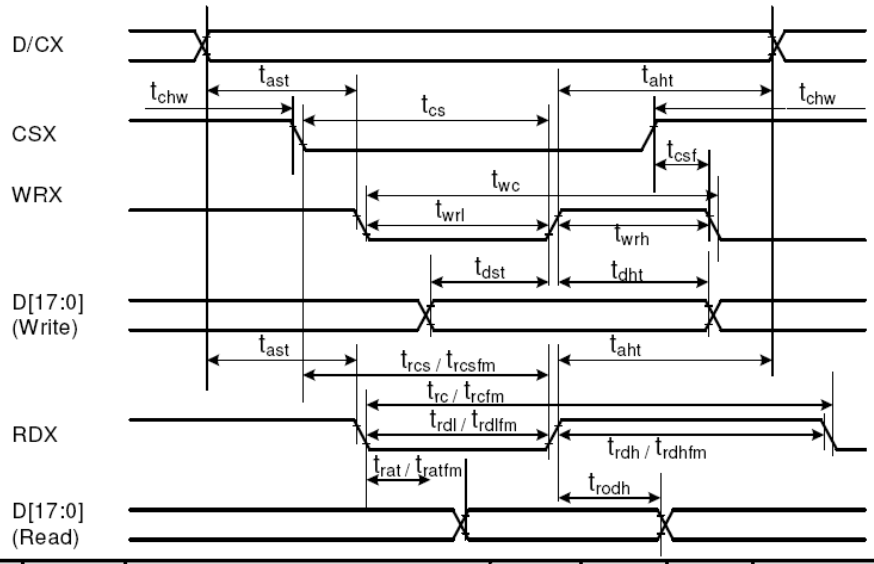


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, AGND=VSS=0V

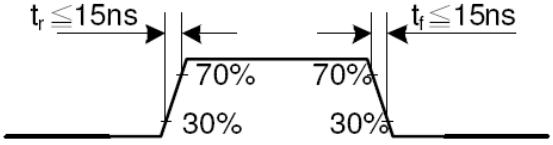


18.3.2 Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)



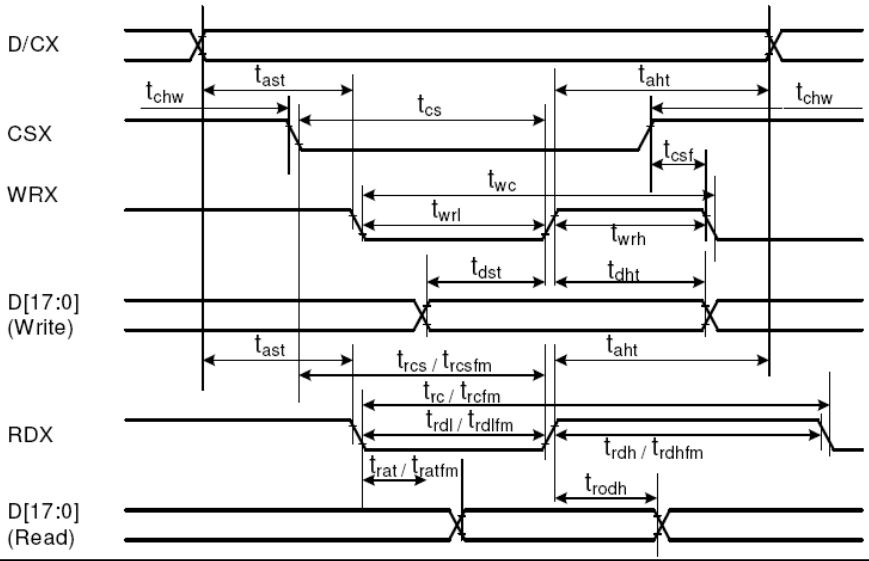
Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.



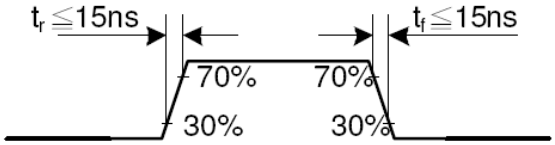
18.3 AC Characteristics

18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V



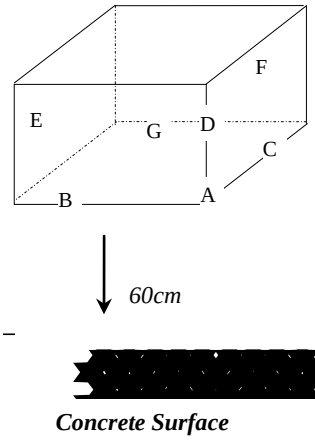
8 Reliability Condition for LCD

No change on display and in operation under the following test condition.

Condition: Unless otherwise specified, tests will be conducted under the following condition.

Temperature: 20±5°C Humidity: 65±5%RH

Tests will be not conducted under functioning state.

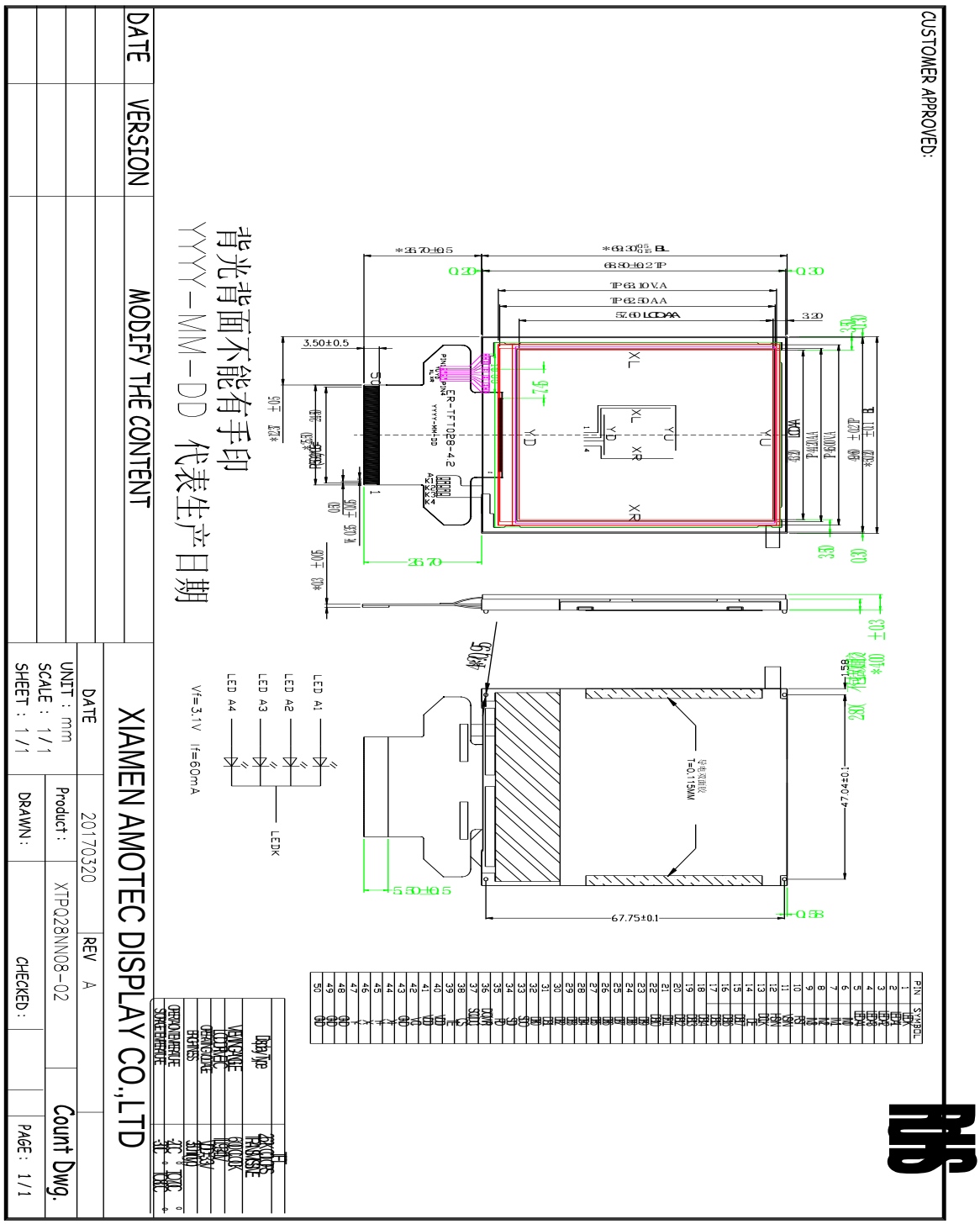
No.	Parameter	Condition	Notes
1	High Temperature Operating	70°C±2°C, 240hrs (Operation state)	--
2	Low Temperature Operating	-20°C±2°C, 240hrs (Operation state)	--
3	High Temperature Storage	80°C±2°C, 240hrs	--
4	Low Temperature Storage	-30°C±2°C, 240hrs	--
5	High Temperature and High Humidity Operation Test	60°C±2°C, 90%, 240hrs	--
6	Vibration Test	Total fixed amplitude: 1.5mm Vibration Frequency: 10~55Hz One cycle 60 seconds to 3 direction of X, Y, Z each 15 minutes.	--
7.	Drop Test	To be measured after dropping from 60cm high on the concrete surface in packing state.  *Dropping method corner dropping* *A corner: once* *Edge dropping* *B, C, D edge: once* *Face dropping* *E, F, G face: once*	--

Notes: 1. No dew condensation to be observed.

2. The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.

3. Vibration test will be conducted to the product itself without putting I in a container.

9 Dimensional outlines



CUSTOMER APPROVED:
背光背面不能有手印
YYYY-MM-DD 代表生产日期
DATE
VERSION
MODIFY THE CONTENT
XIAMEN AMOTEC DISPLAY CO.,LTD
DATE
20170320
REV A
UNIT : mm
SCALE : 1/1
SHEET : 1/1
Product :
XTPQ28NN08-02
DRAWN :
CHECKED :
Count Dwg.
PAGE : 1/1

10 Incoming Inspection Standards

11.1 VISUAL & FUNCTION INSPECTION STANDARD

11.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

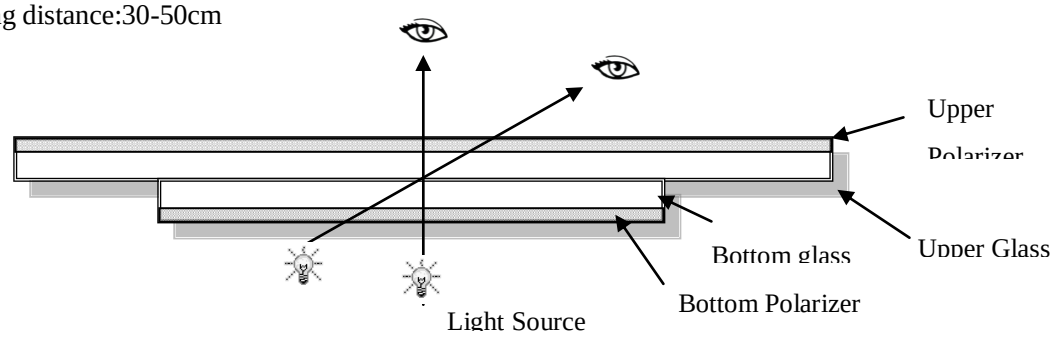
Temperature : 25±5℃

Humidity : 65%±10%RH

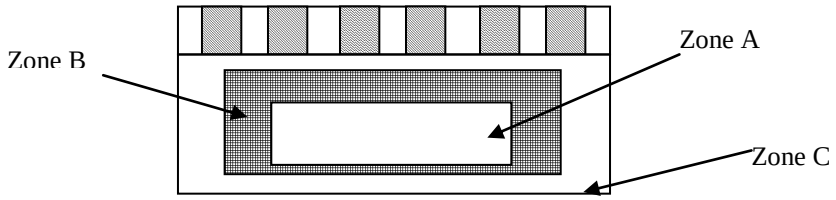
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



11.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Note:

As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer.

11.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

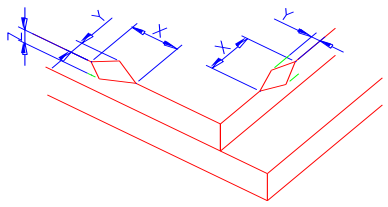
AQL:

Major defect	Minor defect
0.65	1.5

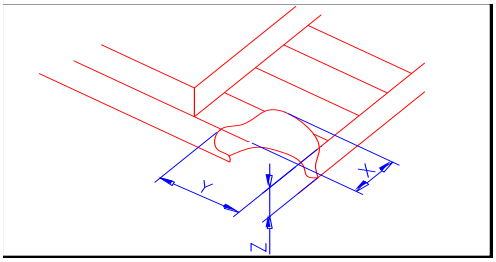
LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

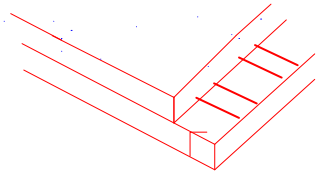
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Soldering appearance	Good soldering , Peeling off is not allowed.	
6	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

11.1.4 Criteria (Visual)

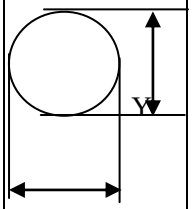
Number	Items	Criteria(mm)
1.0 LCD Crack/Broken NOTE: X: Length Y: Width	(1) The edge of LCD broken	

X	Y	Z
≤3.0mm	<Inner border line of the seal	≤T

<table>
<tr><td rowspan="2">Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(2)LCD corner broken</td><td> 

<table>
<tr><td>X</td><td>Y</td><td>Z</td></tr>
<tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr>
</table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

Number	Items	Criteria (mm)
2.0	Spot defect	① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）



X

Φ=(X+Y)/2

Zone / Size (mm)	Acceptable Qty A	B	C
Φ≤0.10	Ignore		
0.10<Φ≤0.15	3(distance≧10mm)		Ignore
0.15<Φ≤0.2	1		
0.2<Φ	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、 dark spot）

Zone / Size (mm)	Acceptable Qty A	B	C
Φ≤0.1	Ignore		
0.1<Φ≤0.2	2(distance≧10mm)		Ignore
0.2<Φ≤0.3	1		
Φ＞0.3	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty A	B	C
Φ≤0.2	Ignore		
0.2<Φ≤0.5	2(distance≧10mm)		Ignore
Φ>0.5	0		

<table>
<tr>
<td></td>
<td>Line defect (LCD/TP /Polarizer black/white line, scratch, stain)</td>
<td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.05</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.05<W≤0.08</td><td>L≤2.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.08<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>3.0</td>
<td>Polarizer Bubble</td>
<td>
<table>
<tr><td rowspan="2">Zone
Size (mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ<0.2</td><td colspan="2">Ignore</td><td rowspan="4">Ignore</td></tr>
<tr><td>0.2<Φ<0.4</td><td colspan="2">2(distance≧10mm)</td></tr>
<tr><td>0.4<Φ≤0.6</td><td colspan="2">1</td></tr>
<tr><td>0.6<Φ</td><td colspan="2">0</td></tr>
</table>
</td>
</tr>
<tr>
<td>4.0</td>
<td>SMT</td>
<td>According to IPC-A-610C class Ⅱ standard . Function defect and missing part are major defect ,the others are minor defect.</td>
</tr>
</table>